MT6595
Octa-Core Smartphone Application Processor Technical Brief

Version: 0.3
Release date: 2013-12-31

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Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
0.1	2013-10-24	Kelly Teng	
0.2	2013-12-17	Kelly Teng	
0.3	2013-12-31	Kelly Teng	

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1 System Overview

MT6595 is a highly integrated baseband platform incorporating modem and application processing to enable LTE smart phone applications. The chip integrates ARM® Cortex-A17 operating up to 2.2GHz and ARM® Cortex-A7 MPCore™ operating up to 1.7GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. The MT6595 interfaces to LPDDR3 for ultimate performance and also supports booting from eMMC to minimize the overall BOM cost. In addition, an extensive set of interfaces are included to interface to cameras, touch-screen displays, USB3.0, and MMC/SD cards.

The application processor, Quad-core ARM® Cortex-A17 MPCore™ plus Quad-core ARM® Cortex-A7 MPCore™ which equipped with NEON engine, offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 3D graphics acceleration. The multi-standard video codec and an advanced audio subsystem are also integrated to provide advanced multimedia experiences and services such as streaming audio and video, a multitude of decoders and encoders such as HEVC and H264. Audio supports include FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR vocoders, polyphonic ringtones and advanced audio functions such as echo cancellation, hands-free speakerphone operation and active noise cancellation.

An ARM® Cortex-R4, DSP, and 2G and 3G coprocessors provide a powerful modem subsystem capable of supporting LTE Cat 4(150Mbps), Category 24 (42 Mbps) HSDPA downlink and Category 7 (11 Mbps) HSUPA uplink data rates, Category 14 (2.8Mbps) TD-HSDPA downlink and Category 6 (2.2Mbps) TD-HSUPA uplink as well as Class 12 GPRS, EDGE.

The enhanced overall quality is achieved for simultaneous voice, data, and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

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1.1 Platform Features

- **General**
  - Smartphone two MCU subsystems architecture
  - eMMC bootloader

- **AP MCU subsystem**
  - Quad-core ARM® Cortex-A17 MPCore™ operating at 2.2 GHz, 2MB L2 cache
  - Quad-core ARM® Cortex-A7 MPCore™ operating at 1.7 GHz, 512KB L2 cache
  - NEON multimedia processing engine with SIMDv2 / VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - DVFS technology with adaptive operating voltage from 0.8V to 1.15V

- **MD MCU subsystem**
  - ARM® Cortex-R4 processor with maximum 800 MHz operation frequency
  - 64KB I-cache, 64KB D-cache
  - 512KB TCM (tightly-coupled memory)
  - Coresonic DSP for running LTE modem tasks, with maximum 300MHz operation frequency
  - FD216 DSP for running modem/voice tasks, with maximum 250MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control

- **MD external interfaces**
  - Dual SIM/USIM interface supported
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, …)

- **External memory interface**
  - Supports LPDDR3 up to 4GB
  - Dual channel, each with 32-bit data bus width
  - Memory clock up to 933 MHz
  - Supports self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Supports dual rank memory device
  - Advanced bandwidth arbitration control

- **Security**
  - ARM® TrustZone® Security

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- **Connectivity**
  - USB2.0 high-speed dual mode supporting 8 Tx and 8 Rx endpoints
  - USB3.0 device mode.
  - eMMC5.0
  - 4 UARTs for external devices and debugging interfaces
  - SPI master for external devices
  - 5 I2C to control peripheral devices, e.g. CMOS image sensor, or LCM module
  - I2S master output and master/slave input for connection with optional external hi-end audio codec
  - GPIOs
  - 4 sets of memory card controller supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 1.0V
  - Processor DVFS+SRAM voltage : 0.8V~1.15V (Typ. 1.0V ; sleep mode 0.7V)
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V
  - LCM interface: 1.8V
  - Clock source: 26-MHz, 32.768-kHz

- **Package**
  - Type: MWPOP
  - 14mm x 14mm
  - Height: 0.78mm maximum
  - Ball count: Top 256 balls, Bottom 823 balls
  - Ball pitch: Top 0.4mm, Bottom 0.4mm

1.2 MODEM Features

- **LTE**
  - FDD: up to 150 Mbps downlink, 50 Mbps uplink
  - TDD: up to 61 Mbps downlink, 18 Mbps uplink in 20 MHz
  - 1.4 to 20 MHz RF bandwidth
  - 2 × 2 downlink SU-MIMO; 4 × 2 downlink SU-MIMO
  - IPv6, QoS
  - Inter-RAT capabilities with HSPA+, EDGE, and applicable backward-compatible modes
  - SNOW3G/ZUC cipher offload engine

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- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - Two DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - Supports TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data, and packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced sidetone oscillation reduction
  - Digital sidetone generator with programmable gain
  - Two programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering

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- Programmable GSM/GPRS/EDGE modem
- Packet switched data with CS1/CS2/CS3/CS4 coding schemes
- GSM circuit switch data
- GPRS/EDGE Class 12
- Supports SAIC (single antenna interference cancellation) technology
- Supports VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

1.3 Multimedia Features

- **Display**
  - Supports portrait panel resolution up to WQXGA (2560x1600)
  - MIPI DSI interface (8 data lanes)
  - MiraVision™ for picture quality enhancement
  - ClearMotion™ for DTV-class video quality
  - Embedded LCD gamma correction
  - Supports true colors
  - 4 overlay layers with per-pixel alpha channel and gamma table
  - Supports spatial and temporal dithering
  - Supports side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Supports color enhancement
  - Supports adaptive contrast enhancement
  - Supports image/video/graphic sharpness enhancement
  - Supports dynamic backlight scaling
  - Support wide gamut

- **Graphics**
  - OpenGL ES 3.0 3D graphic accelerator capable of processing 150M tri/sec and 2,400M pixel/sec @ 600MHz
  - OpenVG1.1 vector graphics accelerator

- **Image**
  - Integrated image signal processor supports 20 MP
  - Supports electronic image stabilization
  - Supports video stabilization
  - Supports preference color adjustment
  - Supports noise reduction
  - Supports lens shading correction
  - Supports auto sensor defect pixel correction
  - Supports AE/AWB/AF

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- Supports edge enhancement (sharpness)
- Supports face detection and visual tracking
- Supports video face beautify
- Supports zero shutter delay image capture
- Supports capturing full size image when recording video (up to 20M sensor)
- Supports 3 MIPI CSI-2 high-speed camera serial interface, two with 4 data lane (for main) and one with 2 data lane (for sub)
- Hardware JPEG encoder: Baseline encoding with 300M pixel/sec
- Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - HEVC decoder 4k2k @ 30fps
  - VP9 decoder 1080p @ 30fps (SW)
  - H.264 decoder: Baseline 4k2k @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 4k2k@30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 60fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 60fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 60fps/40Mbps
  - VP8 decoder: 1080p @ 60fps/6Mbps
  - VC-1 decoder: 1080p @ 60fps/20Mbps
  - MPEG-4 encoder: Simple profile 1080p @ 30fps (SW)
  - H.263 encoder: 1080 @ 30fps (SW)
  - H.264 encoder: High profile 1080p @ 60fps
  - HEVC encoder: Main profile 4k2k @ 30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 192kHz
  - Audio content sample formats supported: 8-bit/16-bit/24-bit, Mono/Stereo
  - Interfaces supported: I2S, PCM
  - External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz
  - 4-band IIR compensation filter to enhance loudspeaker responses
  - Proprietary audio post-processing technologies: BesLoudness(MB-DRC), Android built-in post processing
  - Audio encode: AMR-NB, AMR-WB, AAC, OGG, ADPCM
  - Audio decode: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM
  - Voice Wakeup
  - 7.1 channel for MHL output

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

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- CTM
- Noise reduction
- Noise suppression
- Noise cancellation
- Dual-MIC noise cancellation
- Echo cancellation
- Echo suppression
- Multi-MIC input (up to 4 MICs)
- Handset mode ANC (active noise reduction)
- Multi-MIC noise cancellation
- Multi-MIC voice tracking
- Multi-MIC sound recording w/t Wind Noise Rejection

1.4 General Descriptions

MediaTek MT6595 is a highly integrated LTE System-on-chip (SoC) which incorporates advanced features e.g. LTE cat.4, Octa HMP core operating at 2.2GHz, 3D graphics (OpenGL|ES 3.0), 20M camera ISP, and LPDDR3-1866 Mbps, WQHD display and 4k2k video codec. MT6595 helps phone manufacturers build high-performance LTE smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

World-leading technology

Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6595 is the brand-new generation smart phone SoC integrating MediaTek LTE modem, Quad-core ARM® Cortex-A7 MPCore™ and ARM® Cortex-A17 MPCore™, 3D graphics and 4k2k video codec.

Rich in features, high-valued product

To enrich the camera features, MT6595 equips a 20M camera ISP with advanced features e.g. auto focus, electrical stabilization, auto sensor defect pixel correction, continuous video AF, face detection, face beautify, burst shot, optical zoom, panorama view and 3D photos.

Incredible browser experience

The powerful big-Little CPU architecture with NEON multimedia processing engine brings PC-like browser experiences while keeps low standby power. GPU which supports OpenGL|ES 3.0 also provides excellent multimedia experiences.

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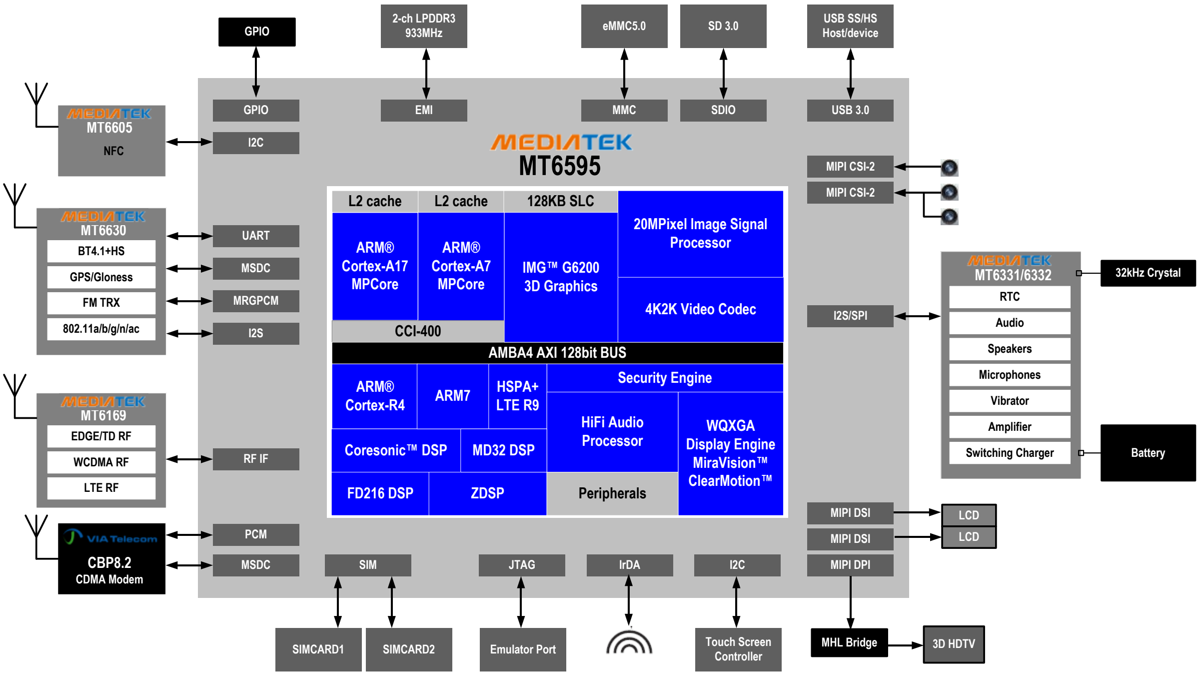

Figure 1-1. Block diagram of MT6595

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

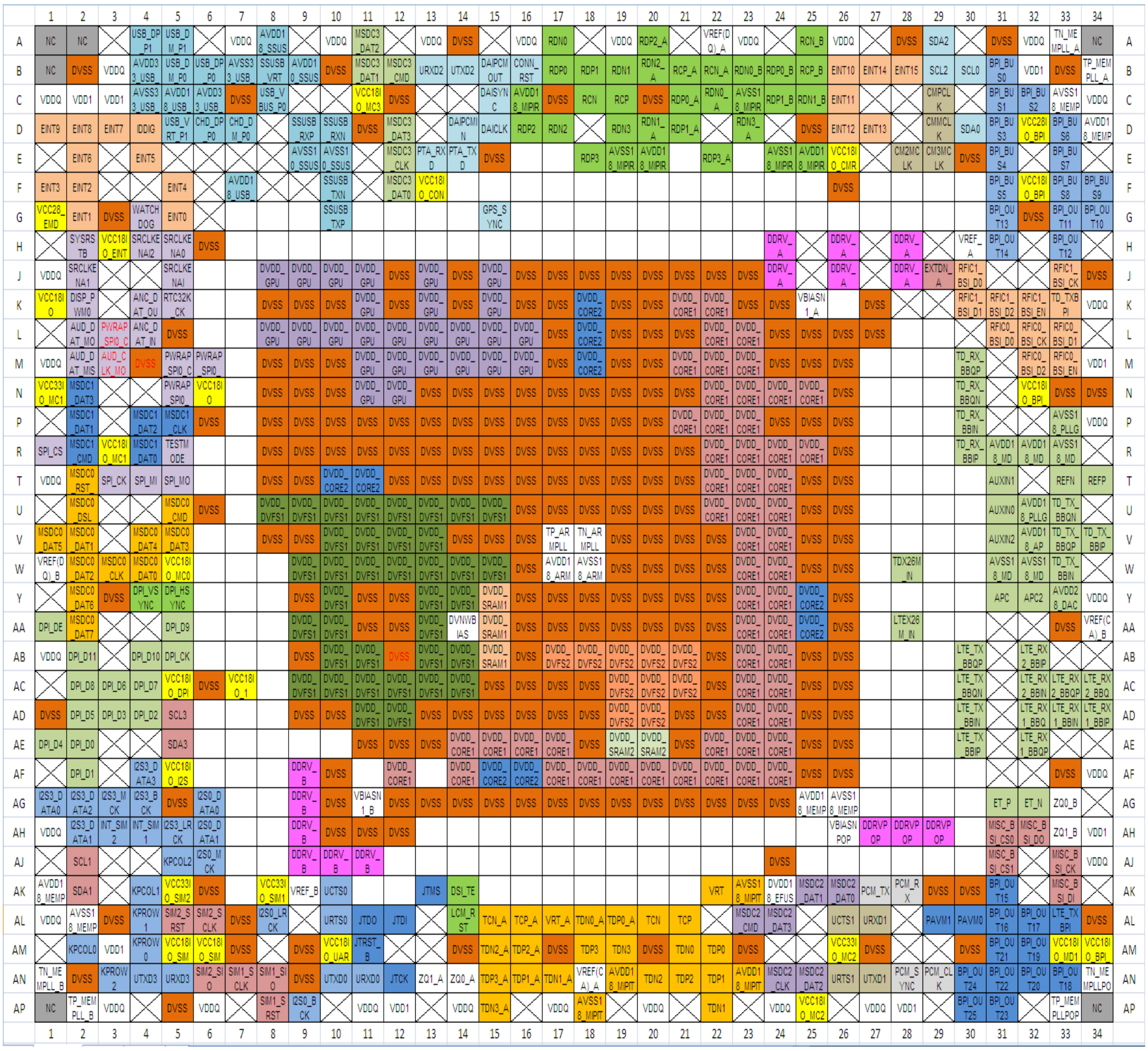

Figure 2-1. Bottom ball map view of MT6595

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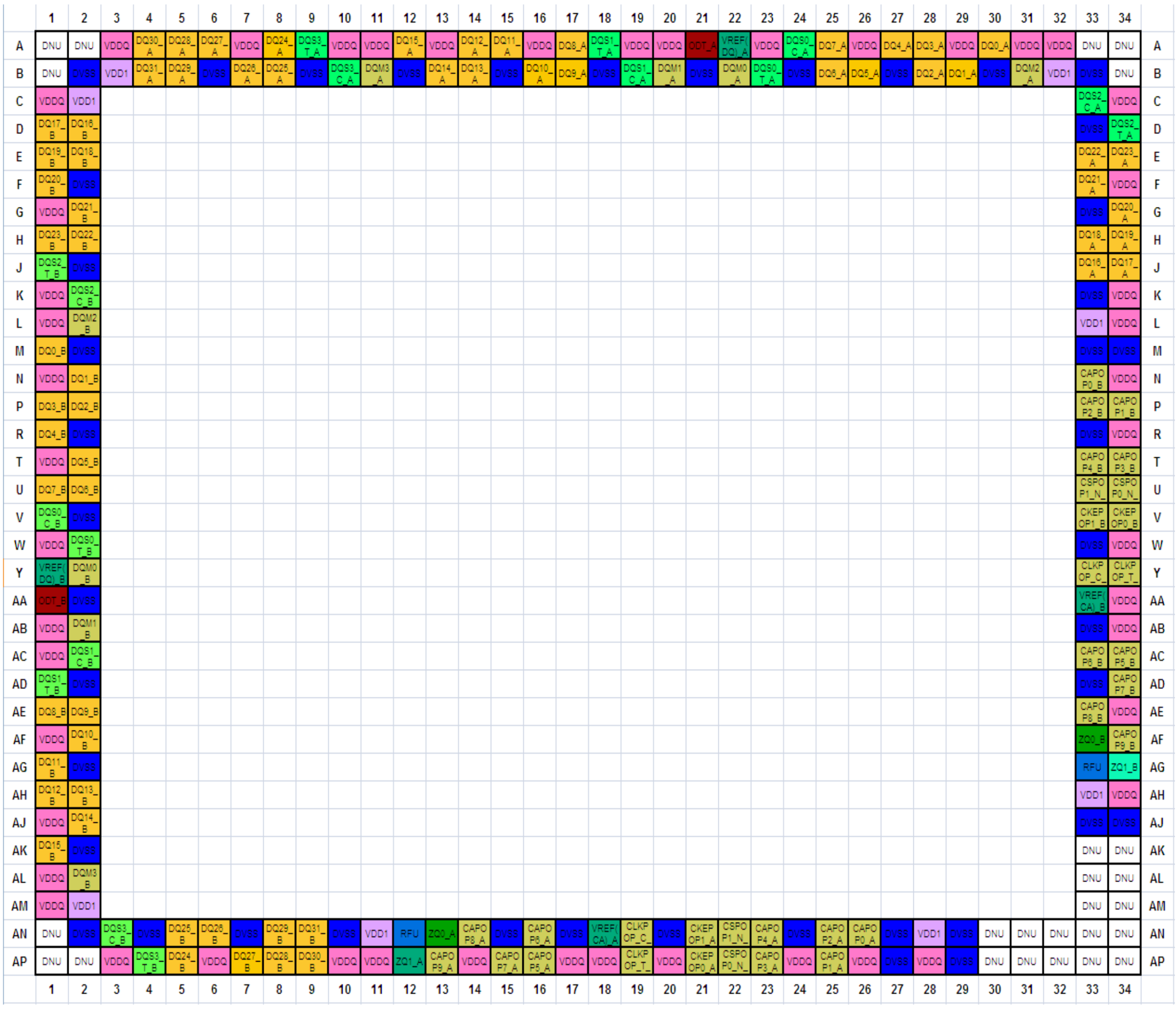

Figure 2-2. Top ball map view of MT6595

2.1.1 Pin Coordinate

Table 2-1. Bottom Pin coordinate

Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
A1	NC	M32	RFIC0_BSI_D2	AC13	DVDD_DVFS1
A2	NC	M33	RFIC0_BSI_EN	AC14	DVDD_DVFS1
A4	USB_DP_P1	M34	VDD1	AC15	DVSS
A5	USB_DM_P1	N1	VCC33IO_MC1	AC16	DVSS
A7	VDDQ	N2	MSDC1_DAT3	AC17	DVSS
A8	AVDD18_SSUSB	N5	PWRAP_SPI0_MO	AC18	DVSS
A10	VDDQ	N6	VCC18IO	AC19	DVDD_DVFS2

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
A11	MSDC3_DAT2	N8	DVSS	AC20	DVDD_DVFS2
A13	VDDQ	N9	DVSS	AC21	DVDD_DVFS2
A14	DVSS	N10	DVSS	AC22	DVSS
A16	VDDQ	N11	DVDD_GPU	AC23	DVDD_CORE1
A17	RDN0	N12	DVDD_GPU	AC24	DVDD_CORE1
A19	VDDQ	N13	DVSS	AC25	DVSS
A20	RDP2_A	N14	DVSS	AC26	DVSS
A22	VREF(DQ)_A	N15	DVSS	AC30	LTE_TX_BBQN
A23	VDDQ	N16	DVSS	AC32	LTE_RX2_BBIN
A25	RCN_B	N17	DVSS	AC33	LTE_RX2_BBQP
A26	VDDQ	N18	DVSS	AC34	LTE_RX2_BBQN
A28	DVSS	N19	DVSS	AD1	DVSS
A29	SDA2	N20	DVSS	AD2	DPI_D5
A31	DVSS	N21	DVSS	AD3	DPI_D3
A32	VDDQ	N22	DVDD_CORE1	AD4	DPI_D2
A33	TN_MEMPLL_A	N23	DVDD_CORE1	AD5	SCL3
A34	NC	N24	DVDD_CORE1	AD9	DVSS
B1	NC	N25	DVDD_CORE1	AD10	DVSS
B2	DVSS	N26	DVSS	AD11	DVDD_DVFS1
B3	VDDQ	N30	TD_RX_BBQN	AD12	DVDD_DVFS1
B4	AVDD33_USB_P1	N32	VCC18IO_BPI_1	AD13	DVSS
B5	USB_DM_P0	N33	DVSS	AD14	DVSS
B6	USB_DP_P0	N34	DVSS	AD15	DVSS
B7	AVSS33_USB_P0	P2	MSDC1_DAT1	AD16	DVSS
B8	SSUSB_VRT	P4	MSDC1_DAT2	AD17	DVSS
B9	AVDD10_SSUSB	P5	MSDC1_CLK	AD18	DVSS
B10	DVSS	P6	DVSS	AD19	DVDD_DVFS2
B11	MSDC3_DAT1	P8	DVSS	AD20	DVDD_DVFS2
B12	MSDC3_CMD	P9	DVSS	AD21	DVSS
B13	URXD2	P10	DVSS	AD22	DVSS
B14	UTXD2	P11	DVSS	AD23	DVDD_CORE1
B15	DAIPCMOUT	P12	DVSS	AD24	DVDD_CORE1
B16	CONN_RST	P13	DVSS	AD25	DVSS
B17	RDP0	P14	DVSS	AD26	DVSS
B18	RDP1	P15	DVSS	AD30	LTE_TX_BBIN
B19	RDN1	P16	DVSS	AD32	LTE_RX1_BBQN
B20	RDN2_A	P17	DVSS	AD33	LTE_RX1_BBIN
B21	RCP_A	P18	DVSS	AD34	LTE_RX1_BBIP

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
B22	RCN_A	P19	DVSS	AE1	DPI_D4
B23	RDN0_B	P20	DVSS	AE2	DPI_D0
B24	RDP0_B	P21	DVDD_CORE1	AE5	SDA3
B25	RCP_B	P22	DVDD_CORE1	AE11	DVSS
B26	EINT10	P23	DVDD_CORE1	AE12	DVSS
B27	EINT14	P24	DVSS	AE13	DVSS
B28	EINT15	P25	DVSS	AE14	DVDD_CORE1
B29	SCL2	P26	DVSS	AE15	DVDD_CORE1
B30	SCL0	P30	TD_RX_BBIN	AE16	DVDD_CORE1
B31	BPI_BUS0	P33	AVSS18_PLLGP	AE17	DVDD_CORE1
B32	VDD1	P34	VDDQ	AE18	DVSS
B33	DVSS	R1	SPI_CS	AE19	DVDD_SRAM2
B34	TP_MEMPLL_A	R2	MSDC1_CMD	AE20	DVDD_SRAM2
C1	VDDQ	R3	VCC18IO_MC1	AE21	DVSS
C2	VDD1	R4	MSDC1_DAT0	AE22	DVDD_CORE1
C3	VDD1	R5	TESTMODE	AE23	DVDD_CORE1
C4	AVSS33_USB_P1	R8	DVSS	AE24	DVDD_CORE1
C5	AVDD18_USB_P1	R9	DVSS	AE25	DVSS
C6	AVDD33_USB_P0	R10	DVSS	AE26	DVSS
C7	DVSS	R11	DVSS	AE30	LTE_TX_BBIP
C8	USB_VBUS_P0	R12	DVSS	AE32	LTE_RX1_BBQP
C11	VCC18IO_MC3	R13	DVSS	AF2	DPI_D1
C12	DVSS	R14	DVSS	AF4	I2S3_DATA3
C15	DAISYNC	R15	DVSS	AF5	VCC18IO_I2S
C16	AVDD18_MIPIRX0	R16	DVSS	AF9	DDRV_B
C17	DVSS	R17	DVSS	AF10	DVSS
C18	RCN	R18	DVSS	AF12	DVDD_CORE1
C19	RCP	R19	DVSS	AF14	DVDD_CORE1
C20	DVSS	R20	DVSS	AF15	DVDD_CORE2
C21	RDP0_A	R21	DVSS	AF16	DVDD_CORE2
C22	RDN0_A	R22	DVDD_CORE1	AF17	DVDD_CORE1
C23	AVSS18_MIPIRX	R23	DVDD_CORE1	AF18	DVDD_CORE1
C24	RDP1_B	R24	DVDD_CORE1	AF19	DVDD_CORE1
C25	RDN1_B	R25	DVDD_CORE1	AF20	DVDD_CORE1
C26	EINT11	R26	DVSS	AF21	DVDD_CORE1
C29	CMPCLK	R30	TD_RX_BBIP	AF22	DVDD_CORE1
C31	BPI_BUS1	R31	AVDD18_MD	AF23	DVDD_CORE1
C32	BPI_BUS2	R32	AVDD18_MD	AF24	DVDD_CORE1

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
C33	AVSS18_MEMPLL_A	R33	AVSS18_MD	AF25	DVSS
C34	VDDQ	T1	VDDQ	AF26	DVSS
D1	EINT9	T2	MSDC0_RST_	AF33	DVSS
D2	EINT8	T3	SPI_CK	AF34	VDDQ
D3	EINT7	T4	SPI_MI	AG1	I2S3_DATA0
D4	IDDIG	T5	SPI_MO	AG2	I2S3_DATA2
D5	USB_VRT_P1	T8	DVSS	AG3	I2S3_MCK
D6	CHD_DP_P0	T9	DVSS	AG4	I2S3_BCK
D7	CHD_DM_P0	T10	DVDD_CORE2	AG5	DVSS
D9	SSUSB_RXP	T11	DVDD_CORE2	AG6	I2S0_DATA0
D10	SSUSB_RXN	T12	DVSS	AG9	DDRV_B
D11	DVSS	T13	DVSS	AG10	DVSS
D12	MSDC3_DAT3	T14	DVSS	AG11	VBIASN1_B
D14	DAIPCMIN	T15	DVSS	AG12	DVSS
D15	DAICLK	T16	DVSS	AG13	DVSS
D16	RDP2	T17	DVSS	AG14	DVSS
D17	RDN2	T18	DVSS	AG15	DVSS
D19	RDN3	T19	DVSS	AG16	DVSS
D20	RDN1_A	T20	DVSS	AG17	DVSS
D21	RDP1_A	T21	DVSS	AG18	DVSS
D23	RDN3_A	T22	DVDD_CORE1	AG19	DVSS
D25	DVSS	T23	DVDD_CORE1	AG20	DVSS
D26	EINT12	T24	DVDD_CORE1	AG21	DVSS
D27	EINT13	T25	DVSS	AG22	DVSS
D29	CMMCLK	T26	DVSS	AG23	DVSS
D30	SDA0	T31	AUXIN1	AG24	DVSS
D31	BPI_BUS3	T33	REFN	AG25	AVDD18_MEMPLLPOP
D32	VCC28IO_BPI	T34	REFP	AG26	AVSS18_MEMPLLPOP
D33	BPI_BUS6	U2	MSDC0_DSL	AG31	ET_P
D34	AVDD18_MEMPLL_A	U5	MSDC0_CMD	AG32	ET_N
E2	EINT6	U6	DVSS	AG33	ZQ0_B
E4	EINT5	U8	DVDD_DVFS1	AH1	VDDQ
E9	AVSS10_SSUSB	U9	DVDD_DVFS1	AH2	I2S3_DATA1
E10	AVSS10_SSUSB	U10	DVDD_DVFS1	AH3	INT_SIM2
E12	MSDC3_CLK	U11	DVDD_DVFS1	AH4	INT_SIM1
E13	PTA_RXD	U12	DVDD_DVFS1	AH5	I2S3_LRCK
E14	PTA_TXD	U13	DVDD_DVFS1	AH6	I2S0_DATA1
E15	DVSS	U14	DVDD_DVFS1	AH9	DDRV_B

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
E18	RDP3	U15	DVDD_DVFS1	AH10	DVSS
E19	AVSS18_MIPIRX	U16	DVSS	AH11	DVSS
E20	AVDD18_MIPIRX1	U17	DVSS	AH12	DVSS
E22	RDP3_A	U18	DVSS	AH26	VBIASNPOP
E24	AVSS18_MIPIRX	U19	DVSS	AH27	DDRVPOP
E25	AVDD18_MIPIRX2	U20	DVSS	AH28	DDRVPOP
E26	VCC18IO_CMR	U21	DVSS	AH29	DDRVPOP
E28	CM2MCLK	U22	DVDD_CORE1	AH31	MISC_BSI_CS0B
E29	CM3MCLK	U23	DVDD_CORE1	AH32	MISC_BSI_DO
E30	DVSS	U24	DVDD_CORE1	AH33	ZQ1_B
E31	BPI_BUS4	U25	DVSS	AH34	VDD1
E33	BPI_BUS7	U26	DVSS	AJ2	SCL1
F1	EINT3	U31	AUXIN0	AJ5	KPCOL2
F2	EINT2	U32	AVDD18_PLLGP	AJ6	I2S0_MCK
F5	EINT4	U33	TD_TX_BBQN	AJ9	DDRV_B
F7	AVDD18_USB_P0	V1	MSDC0_DAT5	AJ10	DDRV_B
F10	SSUSB_TXN	V2	MSDC0_DAT1	AJ11	DDRV_B
F12	MSDC3_DAT0	V4	MSDC0_DAT4	AJ24	DVSS
F13	VCC18IO_CONN	V5	MSDC0_DAT3	AJ31	MISC_BSI_CS1B
F26	DVSS	V8	DVSS	AJ33	MISC_BSI_CK
F31	BPI_BUS5	V9	DVSS	AJ34	VDDQ
F32	VCC18IO_BPI	V10	DVDD_DVFS1	AK1	AVDD18_MEMPLL_B
F33	BPI_BUS8	V11	DVDD_DVFS1	AK2	SDA1
F34	BPI_BUS9	V12	DVDD_DVFS1	AK4	KPCOL1
G1	VCC28_EMD	V13	DVDD_DVFS1	AK5	VCC33IO_SIM2
G2	EINT1	V14	DVSS	AK6	DVSS
G3	DVSS	V15	DVSS	AK8	VCC33IO_SIM1
G4	WATCHDOG	V16	DVSS	AK9	VREF_B
G5	EINT0	V17	TP_ARMPLL	AK10	UCTS0
G10	SSUSB_TXP	V18	TN_ARMPLL	AK13	JTMS
G15	GPS_SYNC	V19	DVSS	AK14	DSI_TE
G31	BPI_OUT13	V20	DVSS	AK22	VRT
G32	DVSS	V21	DVSS	AK23	AVSS18_MIPITX
G33	BPI_OUT11	V22	DVSS	AK24	DVDD18_EFUSE
G34	BPI_OUT10	V23	DVDD_CORE1	AK25	MSDC2_DAT1
H2	SYSRSTB	V24	DVDD_CORE1	AK26	MSDC2_DAT0
H3	VCC18IO_EINT	V25	DVSS	AK27	PCM_TX
H4	SRCLKENAI2	V26	DVSS	AK28	PCM_RX

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
H5	SRCLKENA0	V31	AUXIN2	AK29	DVSS
H6	DVSS	V32	AVDD18_AP	AK30	DVSS
H24	DDRV_A	V33	TD_TX_BBQP	AK31	BPI_OUT15
H26	DDRV_A	V34	TD_TX_BBIP	AK33	MISC_BSI_DI
H28	DDRV_A	W1	VREF(DQ)_B	AL1	VDDQ
H30	VREF_A	W2	MSDC0_DAT2	AL2	AVSS18_MEMPLL_B
H31	BPI_OUT14	W3	MSDC0_CLK	AL3	DVSS
H33	BPI_OUT12	W4	MSDC0_DAT0	AL4	KPROW1
J1	VDDQ	W5	VCC18IO_MC0	AL5	SIM2_SRST
J2	SRCLKENA1	W9	DVDD_DVFS1	AL6	SIM2_SCLK
J5	SRCLKENAI	W10	DVDD_DVFS1	AL7	DVSS
J8	DVDD_GPU	W11	DVDD_DVFS1	AL8	I2S0_LRCK
J9	DVDD_GPU	W12	DVDD_DVFS1	AL10	URTS0
J10	DVDD_GPU	W13	DVDD_DVFS1	AL11	JTDO
J11	DVDD_GPU	W14	DVDD_DVFS1	AL12	JTDI
J12	DVSS	W15	DVDD_DVFS1	AL14	LCM_RST
J13	DVDD_GPU	W16	DVSS	AL15	TCN_A
J14	DVSS	W17	AVDD18_ARMPLL	AL16	TCP_A
J15	DVDD_GPU	W18	AVSS18_ARMPLL	AL17	VRT_A
J16	DVSS	W19	DVSS	AL18	TDN0_A
J17	DVSS	W20	DVSS	AL19	TDP0_A
J18	DVSS	W21	DVSS	AL20	TCN
J19	DVSS	W22	DVSS	AL21	TCP
J20	DVSS	W23	DVDD_CORE1	AL23	MSDC2_CMD
J21	DVSS	W24	DVDD_CORE1	AL24	MSDC2_DAT3
J22	DVSS	W25	DVSS	AL26	UCTS1
J23	DVSS	W26	DVSS	AL27	URXD1
J24	DDRV_A	W28	TDX26M_IN	AL29	PAVM1
J26	DDRV_A	W31	AVSS18_MD	AL30	PAVM0
J28	DDRV_A	W32	AVSS18_MD	AL31	BPI_OUT16
J29	EXTDN_A	W33	TD_TX_BBIN	AL32	BPI_OUT17
J30	RFIC1_BSI_D0	Y2	MSDC0_DAT6	AL33	LTE_TXBPI
J33	RFIC1_BSI_CK	Y3	DVSS	AL34	DVSS
J34	DVSS	Y4	DPI_VSYNC	AM2	KPCOL0
K1	VCC18IO	Y5	DPI_HSYNC	AM3	VDD1
K2	DISP_PWM0	Y9	DVSS	AM4	KPROW0
K4	ANC_DAT_OUT	Y10	DVDD_DVFS1	AM5	VCC18IO_SIM
K5	RTC32K_CK	Y11	DVSS	AM6	VCC18IO_SIM

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
K8	DVSS	Y12	DVSS	AM7	DVSS
K9	DVSS	Y13	DVDD_DVFS1	AM9	DVSS
K10	DVSS	Y14	DVDD_DVFS1	AM10	VCC18IO_UART
K11	DVDD_GPU	Y15	DVDD_SRAM1	AM11	JTRST_B
K12	DVSS	Y16	DVSS	AM14	DVSS
K13	DVDD_GPU	Y17	DVSS	AM15	TDN2_A
K14	DVSS	Y18	DVSS	AM16	TDP2_A
K15	DVDD_GPU	Y19	DVSS	AM17	DVSS
K16	DVSS	Y20	DVSS	AM18	TDP3
K17	DVSS	Y21	DVSS	AM19	TDN3
K18	DVDD_CORE2	Y22	DVSS	AM20	DVSS
K19	DVSS	Y23	DVDD_CORE1	AM21	TDN0
K20	DVSS	Y24	DVDD_CORE1	AM22	TDP0
K21	DVDD_CORE1	Y25	DVDD_CORE2	AM23	DVSS
K22	DVDD_CORE1	Y26	DVSS	AM26	VCC33IO_MC2
K23	DVSS	Y31	APC	AM27	DVSS
K24	DVSS	Y32	APC2	AM30	DVSS
K25	VBIASN1_A	Y33	AVDD28_DAC	AM31	BPI_OUT21
K27	DVSS	Y34	VDDQ	AM32	BPI_OUT19
K30	RFIC1_BSI_D1	AA1	DPI_DE	AM33	VCC18IO_MD1
K31	RFIC1_BSI_D2	AA2	MSDC0_DAT7	AM34	VCC18IO_BPI_2
K32	RFIC1_BSI_EN	AA5	DPI_D9	AN1	TN_MEMPLL_B
K33	TD_TXBPI	AA9	DVDD_DVFS1	AN2	DVSS
K34	VDDQ	AA10	DVDD_DVFS1	AN3	KPROW2
L2	AUD_DAT_MOSI	AA11	DVSS	AN4	UTXD3
L3	PWRAP_SPI0_CSN	AA12	DVSS	AN5	URXD3
L4	ANC_DAT_IN	AA13	DVDD_DVFS1	AN6	SIM2_SIO
L5	DVSS	AA14	DVNWBIAS	AN7	SIM1_SCLK
L8	DVDD_GPU	AA15	DVDD_SRAM1	AN8	SIM1_SIO
L9	DVDD_GPU	AA16	DVSS	AN9	DVSS
L10	DVDD_GPU	AA17	DVSS	AN10	UTXD0
L11	DVDD_GPU	AA18	DVSS	AN11	URXD0
L12	DVDD_GPU	AA19	DVSS	AN12	JTCK
L13	DVDD_GPU	AA20	DVSS	AN13	ZQ1_A
L14	DVDD_GPU	AA21	DVSS	AN14	ZQ0_A
L15	DVDD_GPU	AA22	DVSS	AN15	TDP3_A
L16	DVDD_GPU	AA23	DVDD_CORE1	AN16	TDP1_A
L17	DVSS	AA24	DVDD_CORE1	AN17	TDN1_A

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
L18	DVDD_CORE2	AA25	DVDD_CORE2	AN18	VREF(CA)_A
L19	DVSS	AA26	DVSS	AN19	AVDD18_MIPITX2
L20	DVSS	AA28	LTEX26M_IN	AN20	TDN2
L21	DVSS	AA33	DVSS	AN21	TDP2
L22	DVDD_CORE1	AA34	VREF(CA)_B	AN22	TDP1
L23	DVDD_CORE1	AB1	VDDQ	AN23	AVDD18_MIPITX1
L24	DVSS	AB2	DPI_D11	AN24	MSDC2_CLK
L25	DVSS	AB4	DPI_D10	AN25	MSDC2_DAT2
L26	DVSS	AB5	DPI_CK	AN26	URTS1
L27	DVSS	AB9	DVSS	AN27	UTXD1
L31	RFIC0_BSI_D0	AB10	DVDD_DVFS1	AN28	PCM_SYNC
L32	RFIC0_BSI_CK	AB11	DVDD_DVFS1	AN29	PCM_CLK
L33	RFIC0_BSI_D1	AB12	DVSS	AN30	BPI_OUT24
M1	VDDQ	AB13	DVDD_DVFS1	AN31	BPI_OUT22
M2	AUD_DAT_MISO	AB14	DVDD_DVFS1	AN32	BPI_OUT20
M3	AUD_CLK_MOSI	AB15	DVDD_SRAM1	AN33	BPI_OUT18
M4	DVSS	AB16	DVSS	AN34	TN_MEMPLLPOP
M5	PWRAP_SPI0_CK	AB17	DVDD_DVFS2	AP1	NC
M6	PWRAP_SPI0_MI	AB18	DVDD_DVFS2	AP2	TP_MEMPLL_B
M8	DVSS	AB19	DVDD_DVFS2	AP3	VDDQ
M9	DVSS	AB20	DVDD_DVFS2	AP5	DVSS
M10	DVSS	AB21	DVDD_DVFS2	AP6	VDDQ
M11	DVDD_GPU	AB22	DVSS	AP8	SIM1_SRST
M12	DVDD_GPU	AB23	DVDD_CORE1	AP9	I2S0_BCK
M13	DVDD_GPU	AB24	DVDD_CORE1	AP11	VDDQ
M14	DVDD_GPU	AB25	DVSS	AP12	VDD1
M15	DVDD_GPU	AB26	DVSS	AP14	VDDQ
M16	DVDD_GPU	AB30	LTE_TX_BBQP	AP15	TDN3_A
M17	DVSS	AB32	LTE_RX2_BBIP	AP17	VDDQ
M18	DVDD_CORE2	AC2	DPI_D8	AP18	AVSS18_MIPITX
M19	DVSS	AC3	DPI_D6	AP20	VDDQ
M20	DVSS	AC4	DPI_D7	AP22	TDN1
M21	DVDD_CORE1	AC5	VCC18IO_DPI	AP24	VDDQ
M22	DVDD_CORE1	AC6	DVSS	AP25	VCC18IO_MC2
M23	DVDD_CORE1	AC7	VCC18IO_1	AP27	VDDQ
M24	DVSS	AC9	DVDD_DVFS1	AP28	VDD1
M25	DVSS	AC10	DVDD_DVFS1	AP30	BPI_OUT25
M26	DVSS	AC11	DVDD_DVFS1	AP31	BPI_OUT23

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
M30	TD_RX_BBQP	AC12	DVDD_DVFS1	AP33	TP_MEMPLLPOP
				AP34	NC

Table 2-2. Top pin coordinate

Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
A1	DNU	G2	DQ21_B	AH33	VDD1
A2	DNU	G33	DVSS	AH34	VDDQ
A3	VDDQ	G34	DQ20_A	AJ1	VDDQ
A4	DQ30_A	H1	DQ23_B	AJ2	DQ14_B
A5	DQ28_A	H2	DQ22_B	AJ33	DVSS
A6	DQ27_A	H33	DQ18_A	AJ34	DVSS
A7	VDDQ	H34	DQ19_A	AK1	DQ15_B
A8	DQ24_A	J1	DQS2_T_B	AK2	DVSS
A9	DQS3_T_A	J2	DVSS	AK33	DNU
A10	VDDQ	J33	DQ16_A	AK34	DNU
A11	VDDQ	J34	DQ17_A	AL1	VDDQ
A12	DQ15_A	K1	VDDQ	AL2	DQM3_B
A13	VDDQ	K2	DQS2_C_B	AL33	DNU
A14	DQ12_A	K33	DVSS	AL34	DNU
A15	DQ11_A	K34	VDDQ	AM1	VDDQ
A16	VDDQ	L1	VDDQ	AM2	VDD1
A17	DQ8_A	L2	DQM2_B	AM33	DNU
A18	DQS1_T_A	L33	VDD1	AM34	DNU
A19	VDDQ	L34	VDDQ	AN1	DNU
A20	VDDQ	M1	DQ0_B	AN2	DVSS
A21	ODT_A	M2	DVSS	AN3	DQS3_C_B
A22	VREF(DQ)_A	M33	DVSS	AN4	DVSS
A23	VDDQ	M34	DVSS	AN5	DQ25_B
A24	DQS0_C_A	N1	VDDQ	AN6	DQ26_B
A25	DQ7_A	N2	DQ1_B	AN7	DVSS
A26	VDDQ	N33	CAPOP0_B	AN8	DQ29_B
A27	DQ4_A	N34	VDDQ	AN9	DQ31_B
A28	DQ3_A	P1	DQ3_B	AN10	DVSS
A29	VDDQ	P2	DQ2_B	AN11	VDD1
A30	DQ0_A	P33	CAPOP2_B	AN12	RFU
A31	VDDQ	P34	CAPOP1_B	AN13	ZQ0_A

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
A32	VDDQ	R1	DQ4_B	AN14	CAPOP8_A
A33	DNU	R2	DVSS	AN15	DVSS
A34	DNU	R33	DVSS	AN16	CAPOP6_A
B1	DNU	R34	VDDQ	AN17	DVSS
B2	DVSS	T1	VDDQ	AN18	VREF(CA)_A
B3	VDD1	T2	DQ5_B	AN19	CLKPOP_C_A
B4	DQ31_A	T33	CAPOP4_B	AN20	DVSS
B5	DQ29_A	T34	CAPOP3_B	AN21	CKEPOP1_A
B6	DVSS	U1	DQ7_B	AN22	CSPOP1_N_A
B7	DQ26_A	U2	DQ6_B	AN23	CAPOP4_A
B8	DQ25_A	U33	CSPOP1_N_B	AN24	DVSS
B9	DVSS	U34	CSPOP0_N_B	AN25	CAPOP2_A
B10	DQS3_C_A	V1	DQS0_C_B	AN26	CAPOP0_A
B11	DQM3_A	V2	DVSS	AN27	DVSS
B12	DVSS	V33	CKEPOP1_B	AN28	VDD1
B13	DQ14_A	V34	CKEPOP0_B	AN29	DVSS
B14	DQ13_A	W1	VDDQ	AN30	DNU
B15	DVSS	W2	DQS0_T_B	AN31	DNU
B16	DQ10_A	W33	DVSS	AN32	DNU
B17	DQ9_A	W34	VDDQ	AN33	DNU
B18	DVSS	Y1	VREF(DQ)_B	AN34	DNU
B19	DQS1_C_A	Y2	DQM0_B	AP1	DNU
B20	DQM1_A	Y33	CLKPOP_C_B	AP2	DNU
B21	DVSS	Y34	CLKPOP_T_B	AP3	VDDQ
B22	DQM0_A	AA1	ODT_B	AP4	DQS3_T_B
B23	DQS0_T_A	AA2	DVSS	AP5	DQ24_B
B24	DVSS	AA33	VREF(CA)_B	AP6	VDDQ
B25	DQ6_A	AA34	VDDQ	AP7	DQ27_B
B26	DQ5_A	AB1	VDDQ	AP8	DQ28_B
B27	DVSS	AB2	DQM1_B	AP9	DQ30_B
B28	DQ2_A	AB33	DVSS	AP10	VDDQ
B29	DQ1_A	AB34	VDDQ	AP11	VDDQ
B30	DVSS	AC1	VDDQ	AP12	ZQ1_A
B31	DQM2_A	AC2	DQS1_C_B	AP13	CAPOP9_A
B32	VDD1	AC33	CAPOP6_B	AP14	VDDQ
B33	DVSS	AC34	CAPOP5_B	AP15	CAPOP7_A
B34	DNU	AD1	DQS1_T_B	AP16	CAPOP5_A
C1	VDDQ	AD2	DVSS	AP17	VDDQ

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
C2	VDD1	AD33	DVSS	AP18	VDDQ
C33	DQS2_C_A	AD34	CAPOP7_B	AP19	CLKPOP_T_A
C34	VDDQ	AE1	DQ8_B	AP20	VDDQ
D1	DQ17_B	AE2	DQ9_B	AP21	CKEPOP0_A
D2	DQ16_B	AE33	CAPOP8_B	AP22	CSPOP0_N_A
D33	DVSS	AE34	VDDQ	AP23	CAPOP3_A
D34	DQS2_T_A	AF1	VDDQ	AP24	VDDQ
E1	DQ19_B	AF2	DQ10_B	AP25	CAPOP1_A
E2	DQ18_B	AF33	ZQ0_B	AP26	VDDQ
E33	DQ22_A	AF34	CAPOP9_B	AP27	DVSS
E34	DQ23_A	AG1	DQ11_B	AP28	VDDQ
F1	DQ20_B	AG2	DVSS	AP29	DVSS
F2	DVSS	AG33	RFU	AP30	DNU
F33	DQ21_A	AG34	ZQ1_B	AP31	DNU
F34	VDDQ	AH1	DQ12_B	AP32	DNU
G1	VDDQ	AH2	DQ13_B	AP33	DNU
				AP34	DNU

2.1.2 Detailed Pin Description

Table 2-3. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 2-4. Detailed pin description

Pin name	Type	Description	Power domain
SYSTEM			
SYSRSTB	DIO	System reset input	VCC18IO
WATCHDOG	DIO	Watchdog reset output	VCC18IO
TESTMODE	DIO	Test mode	VCC18IO
SRCLKENA0	DIO	26MHz co-clock enable output	VCC18IO

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Pin name	Type	Description	Power domain
SRCLKENA1	DIO	26MHz co-clock enable output	VCC18IO
SRCLKENAI	DIO	26MHz co-clock enable input	VCC18IO
SRCLKENAI2	DIO	26MHz co-clock enable input	VCC18IO
RTC32K_CK	DIO	32K clock input	VCC18IO
PMIC			
PWRAP_SPI0_CK	DIO	PMIC SPI control interface	VCC18IO
PWRAP_SPI0_CSN	DIO	PMIC SPI control interface	VCC18IO
PWRAP_SPI0_MI	DIO	PMIC SPI control interface	VCC18IO
PWRAP_SPI0_MO	DIO	PMIC SPI control interface	VCC18IO
AUD_CLK_MOSI	DIO	PMIC audio input interface	VCC18IO
AUD_DAT_MISO	DIO	PMIC audio input interface	VCC18IO
AUD_DAT_MOSI	DIO	PMIC audio input interface	VCC18IO
ANC_DAT_IN	DIO	PMIC audio input interface	VCC18IO
ANC_DAT_OUT	DIO	PMIC audio input interface	VCC18IO
SIM			
SIM1_SCLK	DIO	SIM1 CLOCK	VCC18IO_SIM/VCC33IO_SIM1
SIM1_SIO	DIO	SIM1 DATA	VCC18IO_SIM/VCC33IO_SIM1
SIM1_SRST	DIO	SIM1 RST	VCC18IO_SIM/VCC33IO_SIM1
SIM2_SCLK	DIO	SIM2 CLOCK	VCC18IO_SIM/VCC33IO_SIM2
SIM2_SIO	DIO	SIM2 DATA	VCC18IO_SIM/VCC33IO_SIM2
SIM2_SRST	DIO	SIM2 RST	VCC18IO_SIM/VCC33IO_SIM2
INT_SIM1	DIO	SIM1 INT	VCC18IO
INT_SIM2	DIO	SIM2 INT	VCC18IO
JTAG			
JTCK	DIO	JTCK	VCC18IO_UART
JTDI	DIO	JTDI	VCC18IO_UART
JTDO	DIO	JTDO	VCC18IO_UART
JTMS	DIO	JTMS	VCC18IO_UART
JTRST_B	DIO	JTRST	VCC18IO_UART
LCD			
DISP_PWM0	DIO	Display PWM output	VCC18IO
DSI_TE	DIO	Parallel display interface tearing effect	VCC18IO_UART
LCM_RST	DIO	Parallel display interface reset signal	VCC18IO_UART
I2S			
I2S0_BCK	DIO	I2S bi-directional interfece	VCC18IO_UART
I2S0_DATA0	DIO	I2S bi-directional interfece	VCC18IO_UART
I2S0_DATA1	DIO	I2S bi-directional interfece	VCC18IO_UART
I2S0_LRCK	DIO	I2S bi-directional interfece	VCC18IO_UART
I2S0_MCK	DIO	I2S bi-directional interfece	VCC18IO_UART
I2S3_BCK	DIO	I2S output	VCC18IO_I2S
I2S3_DATA0	DIO	I2S output	VCC18IO_I2S
I2S3_DATA1	DIO	I2S output	VCC18IO_I2S
I2S3_DATA2	DIO	I2S output	VCC18IO_I2S
I2S3_DATA3	DIO	I2S output	VCC18IO_I2S

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Pin name	Type	Description	Power domain
I2S3_LRCK	DIO	I2S output	VCC18IO_I2S
I2S3_MCK	DIO	I2S output	VCC18IO_I2S
PCM/I2S merge interface			
PCM_CLK	DIO	PCM audio interface	VCC18IO_MC2
PCM_RX	DIO	PCM audio interface	VCC18IO_MC2
PCM_SYNC	DIO	PCM audio interface	VCC18IO_MC2
PCM_TX	DIO	PCM audio interface	VCC18IO_MC2
EINT			
EINT0	DIO	External interrupt 0	VCC18IO_EINT/VCC28_EMD
EINT1	DIO	External interrupt 1	VCC18IO_EINT/VCC28_EMD
EINT2	DIO	External interrupt 2	VCC18IO_EINT/VCC28_EMD
EINT3	DIO	External interrupt 3	VCC18IO_EINT/VCC28_EMD
EINT4	DIO	External interrupt 4	VCC18IO_EINT/VCC28_EMD
EINT5	DIO	External interrupt 5	VCC18IO_EINT/VCC28_EMD
EINT6	DIO	External interrupt 6	VCC18IO_EINT/VCC28_EMD
EINT7	DIO	External interrupt 7	VCC18IO_EINT/VCC28_EMD
EINT8	DIO	External interrupt 8	VCC18IO_EINT/VCC28_EMD
EINT9	DIO	External interrupt 9	VCC18IO_EINT/VCC28_EMD
EINT10	DIO	External interrupt 10	VCC18IO_CMR
EINT11	DIO	External interrupt 11	VCC18IO_CMR
EINT12	DIO	External interrupt 12	VCC18IO_CMR
EINT13	DIO	External interrupt 13	VCC18IO_CMR
EINT14	DIO	External interrupt 14	VCC18IO_CMR
EINT15	DIO	External interrupt 15	VCC18IO_CMR
SPI			
SPI_CK	DIO	SPI clock	VCC18IO
SPI_CS	DIO	SPI chip select	VCC18IO
SPI_MI	DIO	SPI master data in	VCC18IO
SPI_MO	DIO	SPI master data out	VCC18IO
BPI			
BPI_BUS0	DIO	BPI1 BUS0	VCC18IO_BPI/VCC28IO_BPI
BPI_BUS1	DIO	BPI1 BUS1	VCC18IO_BPI/VCC28IO_BPI
BPI_BUS2	DIO	BPI1 BUS2	VCC18IO_BPI/VCC28IO_BPI
BPI_BUS3	DIO	BPI1 BUS3	VCC18IO_BPI/VCC28IO_BPI
BPI_BUS4	DIO	BPI1 BUS4	VCC18IO_BPI/VCC28IO_BPI
BPI_BUS5	DIO	BPI1 BUS5	VCC18IO_BPI/VCC28IO_BPI
BPI_BUS6	DIO	BPI1 BUS6	VCC18IO_BPI/VCC28IO_BPI
BPI_BUS7	DIO	BPI1 BUS7	VCC18IO_BPI/VCC28IO_BPI
BPI_BUS8	DIO	BPI1 BUS8	VCC18IO_BPI/VCC28IO_BPI
BPI_BUS9	DIO	BPI1 BUS9	VCC18IO_BPI/VCC28IO_BPI
BPI_OUT10	DIO	BPI1 OUT10	VCC18IO_BPI_1
BPI_OUT11	DIO	BPI1 OUT11	VCC18IO_BPI_1
BPI_OUT12	DIO	BPI1 OUT12	VCC18IO_BPI_1
BPI_OUT13	DIO	BPI1 OUT13	VCC18IO_BPI_1

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Pin name	Type	Description	Power domain
BPI_OUT14	DIO	BPI1 OUT14	VCC18IO_BPI_1
BPI_OUT15	DIO	BPI1 OUT15	VCC18IO_BPI_2
BPI_OUT16	DIO	BPI1 OUT16	VCC18IO_BPI_2
BPI_OUT17	DIO	BPI1 OUT17	VCC18IO_BPI_2
BPI_OUT18	DIO	BPI1 OUT18	VCC18IO_BPI_2
BPI_OUT19	DIO	BPI1 OUT19	VCC18IO_BPI_2
BPI_OUT20	DIO	BPI1 OUT20	VCC18IO_BPI_2
BPI_OUT21	DIO	BPI1 OUT21	VCC18IO_BPI_2
BPI_OUT22	DIO	BPI1 OUT22	VCC18IO_BPI_2
BPI_OUT23	DIO	BPI1 OUT23	VCC18IO_BPI_2
BPI_OUT24	DIO	BPI1 OUT24	VCC18IO_BPI_2
BPI_OUT25	DIO	BPI1 OUT25	VCC18IO_BPI_2
VM			
PAVM0	DIO	PA mode selection	VCC18IO_BPI_2
PAVM1	DIO	PA mode selection	VCC18IO_BPI_2
BSI			
RFIC0_BSI_D0	DIO	RFIC0 BSI DATA0	VCC18IO_BPI_1
RFIC0_BSI_D1	DIO	RFIC0 BSI DATA1	VCC18IO_BPI_1
RFIC0_BSI_D2	DIO	RFIC0 BSI DATA2	VCC18IO_BPI_1
RFIC0_BSI_EN	DIO	RFIC0 BSI CS0	VCC18IO_BPI_1
RFIC0_BSI_CK	DIO	RFIC0 BSI CLK	VCC18IO_BPI_1
RFIC1_BSI_CK	DIO	RFIC1 BSI CLK	VCC18IO_BPI_1
RFIC1_BSI_D0	DIO	RFIC1 BSI DATA0	VCC18IO_BPI_1
RFIC1_BSI_D1	DIO	RFIC1 BSI DATA1	VCC18IO_BPI_1
RFIC1_BSI_D2	DIO	RFIC1 BSI DATA2	VCC18IO_BPI_1
RFIC1_BSI_EN	DIO	RFIC1 BSI CS0	VCC18IO_BPI_1
MISC_BSI_CK	DIO	MISC BSI CLK	VCC18IO_MD1
MISC_BSI_CS0B	DIO	MISC BSI CS0	VCC18IO_MD1
MISC_BSI_CS1B	DIO	MISC BSI CS1	VCC18IO_MD1
MISC_BSI_DI	DIO	MISC BSI DATAI	VCC18IO_MD1
MISC_BSI_DO	DIO	MISC BSI DATAO	VCC18IO_MD1
TD_TXBPI	DIO	TXBPI	VCC18IO_BPI_1
LTE_TXBPI	DIO	TXBPI	VCC18IO_BPI_2
MSDC0			
MSDC0_CLK	DIO	MSDC0 CLK	VCC18IO_MC0
MSDC0_CMD	DIO	MSDC0 CMD	VCC18IO_MC0
MSDC0_DAT0	DIO	MSDC0 data0 pin	VCC18IO_MC0
MSDC0_DAT1	DIO	MSDC0 data1 pin	VCC18IO_MC0
MSDC0_DAT2	DIO	MSDC0 data2 pin	VCC18IO_MC0
MSDC0_DAT3	DIO	MSDC0 data3 pin	VCC18IO_MC0
MSDC0_DAT4	DIO	MSDC0 data4 pin	VCC18IO_MC0
MSDC0_DAT5	DIO	MSDC0 data5 pin	VCC18IO_MC0
MSDC0_DAT6	DIO	MSDC0 data6 pin	VCC18IO_MC0
MSDC0_DAT7	DIO	MSDC0 data7 pin	VCC18IO_MC0

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Pin name	Type	Description	Power domain
MSDC0_DSL	DIO	MSDC0 DSL	VCC18IO_MC0
MSDC0_RST_	DIO	MSDC0 RST	VCC18IO_MC0
MSDC1			
MSDC1_CLK	DIO	MSDC1 clock output	VCC18IO_MC1
MSDC1_CMD	DIO	MSDC1 command pin	VCC18IO_MC1
MSDC1_DAT0	DIO	MSDC1 data0 pin	VCC18IO_MC1
MSDC1_DAT1	DIO	MSDC1 data1 pin	VCC18IO_MC1
MSDC1_DAT2	DIO	MSDC1 data2 pin	VCC18IO_MC1
MSDC1_DAT3	DIO	MSDC1 data3 pin	VCC18IO_MC1
MSDC2			
MSDC2_CLK	DIO	MSDC2 clock output	VCC18IO_MC2/VCC33IO_MC2
MSDC2_CMD	DIO	MSDC2 command pin	VCC18IO_MC2/VCC33IO_MC2
MSDC2_DAT0	DIO	MSDC2 data0 pin	VCC18IO_MC2/VCC33IO_MC2
MSDC2_DAT1	DIO	MSDC2 data1 pin	VCC18IO_MC2/VCC33IO_MC2
MSDC2_DAT2	DIO	MSDC2 data2 pin	VCC18IO_MC2/VCC33IO_MC2
MSDC2_DAT3	DIO	MSDC2 data3 pin	VCC18IO_MC2/VCC33IO_MC2
MSDC3			
MSDC3_CLK	DIO	MSDC3 clock output	VCC18IO_MC3
MSDC3_CMD	DIO	MSDC3 command pin	VCC18IO_MC3
MSDC3_DAT0	DIO	MSDC3 data0 pin	VCC18IO_MC3
MSDC3_DAT1	DIO	MSDC3 data1 pin	VCC18IO_MC3
MSDC3_DAT2	DIO	MSDC3 data2 pin	VCC18IO_MC3
MSDC3_DAT3	DIO	MSDC3 data3 pin	VCC18IO_MC3
CAM			
CM2MCLK	DIO	Digital Camera Interface	VCC18IO_CMR
CM3MCLK	DIO	Digital Camera Interface	VCC18IO_CMR
CMMCLK	DIO	Digital Camera Interface	VCC18IO_CMR
CMPCLK	DIO	Digital Camera Interface	VCC18IO_CMR
I2C			
SCL0	DIO	I2C0 clock	VCC18IO_CMR
SDA0	DIO	I2C0 data	VCC18IO_CMR
SCL1	DIO	I2C1 clock	VCC18IO
SDA1	DIO	I2C1 data	VCC18IO
SCL2	DIO	I2C2 clock	VCC18IO_CMR
SDA2	DIO	I2C2 data	VCC18IO_CMR
SCL3	DIO	I2C3 clock	VCC18IO_I2S
SDA3	DIO	I2C3 data	VCC18IO_I2S
UART			
UCTS0	DIO	UART0 CTS	VCC18IO_UART
URTS0	DIO	UART0 RTS	VCC18IO_UART
URXD0	DIO	UART0 RX	VCC18IO_UART
UTXD0	DIO	UART0 TX	VCC18IO_UART
UCTS1	DIO	UART1 CTS	VCC18IO_MC2
URTS1	DIO	UART1 RTS	VCC18IO_MC2

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Pin name	Type	Description	Power domain
URXD1	DIO	UART1 RX	VCC18IO_MC2
UTXD1	DIO	UART1 TX	VCC18IO_MC2
URXD2	DIO	UART2 RX	VCC18IO_CONN
UTXD2	DIO	UART2 TX	VCC18IO_CONN
URXD3	DIO	UART3 RX	VCC18IO
UTXD3	DIO	UART3 TX	VCC18IO
PTA_RXD	DIO	UART PTA RDX	VCC18IO_CONN
PTA_TXD	DIO	UART PTA TDX	VCC18IO_CONN
KeyPad			
KPCOL0	DIO	Keypad COL0	VCC18IO
KPCOL1	DIO	Keypad COL1	VCC18IO
KPCOL2	DIO	Keypad COL2	VCC18IO
KPROW0	DIO	Keypad ROW0	VCC18IO
KPROW1	DIO	Keypad ROW0	VCC18IO
KPROW2	DIO	Keypad ROW0	VCC18IO
MISC			
IDDIG	DIO	IDDIG	VCC18IO
CONN_RST	DIO	Connect SYS Reset	VCC18IO_CONN
GPS_SYNC	DIO	GPS SYNC	VCC18IO_CONN
DAI Merged Interface			
DAICLK	DIO	DAI Audio interface	VCC18IO_CONN
DAIPCMIN	DIO	DAI Audio interface	VCC18IO_CONN
DAIPCMOUT	DIO	DAI Audio interface	VCC18IO_CONN
DAISYNC	DIO	DAI Audio interface	VCC18IO_CONN
DPI			
DPI_CK	DIO	DPI clock	VCC18IO_DPI
DPI_D0	DIO	DPI data0	VCC18IO_DPI
DPI_D1	DIO	DPI data1	VCC18IO_DPI
DPI_D2	DIO	DPI data2	VCC18IO_DPI
DPI_D3	DIO	DPI data3	VCC18IO_DPI
DPI_D4	DIO	DPI data4	VCC18IO_DPI
DPI_D5	DIO	DPI data5	VCC18IO_DPI
DPI_D6	DIO	DPI data6	VCC18IO_DPI
DPI_D7	DIO	DPI data7	VCC18IO_DPI
DPI_D8	DIO	DPI data8	VCC18IO_DPI
DPI_D9	DIO	DPI data9	VCC18IO_DPI
DPI_D10	DIO	DPI data10	VCC18IO_DPI
DPI_D11	DIO	DPI data11	VCC18IO_DPI
DPI_DE	DIO	DPI data enable	VCC18IO_DPI
DPI_HSYNC	DIO	DPI HSYNC	VCC18IO_DPI
DPI_VSYNC	DIO	DPI VSYNC	VCC18IO_DPI
ABB			
APC	AIO	Automatic power control for MD1	AVDD28_DAC
APC2	AIO	Automatic power control for MD2	AVDD28_DAC

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Pin name	Type	Description	Power domain
AUXIN0	AIO	AuxADC external input channel 0	AVDD18_AP
AUXIN1	AIO	AuxADC external input channel 1	AVDD18_AP
AUXIN2	AIO	AuxADC external input channel 2	AVDD18_AP
ET_N	AIO	Envelop Tracking DAC output P	AVDD18_MD
ET_P	AIO	Envelop Tracking DAC output N	AVDD18_MD
LTE_RX1_BBIN	AIO	LTE downlink IN for main path	AVDD18_MD
LTE_RX1_BBIP	AIO	LTE downlink IP for main path	AVDD18_MD
LTE_RX1_BBQN	AIO	LTE downlink QN for main path	AVDD18_MD
LTE_RX1_BBQP	AIO	LTE downlink QP for main path	AVDD18_MD
LTE_RX2_BBIN	AIO	LTE downlink IN for diversity path	AVDD18_MD
LTE_RX2_BBIP	AIO	LTE downlink IP for diversity path	AVDD18_MD
LTE_RX2_BBQN	AIO	LTE downlink QN for diversity path	AVDD18_MD
LTE_RX2_BBQP	AIO	LTE downlink QP for diversity path	AVDD18_MD
LTE_TX_BBIN	AIO	LTE uplink IN	AVDD18_MD
LTE_TX_BBIP	AIO	LTE uplink IP	AVDD18_MD
LTE_TX_BBQN	AIO	LTE uplink QN	AVDD18_MD
LTE_TX_BBQP	AIO	LTE uplink QP	AVDD18_MD
LTEX26M_IN	AIO	26MHz clock input for AP & 1st modem	AVDD18_MD
REFN	AIO	Negative reference port for internal circuit	AVDD18_AP
REFP	AIO	Positive reference port for internal circuit	AVDD18_AP
TD_RX_BBIN	AIO	2nd modem downlink IN	AVDD18_MD
TD_RX_BBIP	AIO	2nd modem downlink IP	AVDD18_MD
TD_RX_BBQN	AIO	2nd modem downlink QN	AVDD18_MD
TD_RX_BBQP	AIO	2nd modem downlink QP	AVDD18_MD
TD_TX_BBIN	AIO	2nd modem uplink IN	AVDD18_MD
TD_TX_BBIP	AIO	2nd modem uplink IP	AVDD18_MD
TD_TX_BBQN	AIO	2nd modem uplink QN	AVDD18_MD
TD_TX_BBQP	AIO	2nd modem uplink QP	AVDD18_MD
TDX26M_IN	AIO	26MHz clock input for 2nd modem	AVDD18_MD
MIPIRX			
RDN3	AIO	CSI0 lane3 N	AVDD18_MIPIRX0
RDP3	AIO	CSI0 lane3 P	AVDD18_MIPIRX0
RDN2	AIO	CSI0 lane2 N	AVDD18_MIPIRX0
RDP2	AIO	CSI0 lane2 P	AVDD18_MIPIRX0
RCN	AIO	CSI0 CK lane N	AVDD18_MIPIRX0
RCP	AIO	CSI0 CK lane P	AVDD18_MIPIRX0
RDN1	AIO	CSI0 lane1 N	AVDD18_MIPIRX0
RDP1	AIO	CSI0 lane1 P	AVDD18_MIPIRX0
RDN0	AIO	CSI0 lane0 N	AVDD18_MIPIRX0
RDP0	AIO	CSI0 lane0 P	AVDD18_MIPIRX0
RDN3_A	AIO	CSI1 lane3 N	AVDD18_MIPIRX1
RDP3_A	AIO	CSI1 lane3 P	AVDD18_MIPIRX1
RDN2_A	AIO	CSI1 lane2 N	AVDD18_MIPIRX1
RDP2_A	AIO	CSI1 lane2 P	AVDD18_MIPIRX1

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Pin name	Type	Description	Power domain
RCN_A	AIO	CSI1 CK lane N	AVDD18_MIPIRX1
RCP_A	AIO	CSI1 CK lane P	AVDD18_MIPIRX1
RDN1_A	AIO	CSI1 lane1 N	AVDD18_MIPIRX1
RDP1_A	AIO	CSI1 lane1 P	AVDD18_MIPIRX1
RDN0_A	AIO	CSI1 lane0 N	AVDD18_MIPIRX1
RDP0_A	AIO	CSI1 lane0 P	AVDD18_MIPIRX1
RCN_B	AIO	CSI2 CK lane N	AVDD18_MIPIRX2
RCP_B	AIO	CSI2 CK lane P	AVDD18_MIPIRX2
RDN1_B	AIO	CSI2 lane1 N	AVDD18_MIPIRX2
RDP1_B	AIO	CSI2 lane1 P	AVDD18_MIPIRX2
RDN0_B	AIO	CSI2 lane0 N	AVDD18_MIPIRX2
RDP0_B	AIO	CSI2 lane0 P	AVDD18_MIPIRX2
USB2			
USB_DP_P0	AIO	USB port0 D+ differential data line	AVDD33_USB
USB_DM_P0	AIO	USB port0 D- differential data line	AVDD33_USB
USB_DP_P1	AIO	USB port1 D+ differential data line	AVDD33_USB
USB_DM_P1	AIO	USB port1 D- differential data line	AVDD33_USB
USB_VBUS_P0	AIO	USB port0 VBUS	AVDD18_USB
USB_VRT_P1	AIO	USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD18_USB
CHD_DM_P0	AIO	BC1.1 Charger DM	AVDD33_USB
CHD_DP_P0	AIO	BC1.1 Charger DP	AVDD33_USB
USB3			
SSUSB_RXN	AIO	SSUSBRXDATA	AVDD10_SSUSB
SSUSB_RXP	AIO	SSUSBRXDATA	AVDD10_SSUSB
SSUSB_TXN	AIO	SSUSBTXDATA	AVDD10_SSUSB
SSUSB_TXP	AIO	SSUSBTXDATA	AVDD10_SSUSB
SSUSB_VRT	AIO	USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD18_USB
MIPITX			
TDN3	AIO	DSI0 lane3 N	AVDD18_MIPITX1
TDP3	AIO	DSI0 lane3 P	AVDD18_MIPITX1
TDN2	AIO	DSI0 lane2 N	AVDD18_MIPITX1
TDP2	AIO	DSI0 lane2 P	AVDD18_MIPITX1
TCN	AIO	DSI0 CK lane N	AVDD18_MIPITX1
TCP	AIO	DSI0 CK lane P	AVDD18_MIPITX1
TDN1	AIO	DSI0 lane1 N	AVDD18_MIPITX1
TDP1	AIO	DSI0 lane1 P	AVDD18_MIPITX1
TDN0	AIO	DSI0 lane0 N	AVDD18_MIPITX1
TDP0	AIO	DSI0 lane0 P	AVDD18_MIPITX1
VRT	AO	External resistor for DSI0 bias Connect 1.5K ohm 1% resistor to ground	AVDD18_MIPITX1
TDN3_A	AIO	DSI1 lane3 N	AVDD18_MIPITX2
TDP3_A	AIO	DSI1 lane3 P	AVDD18_MIPITX2

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Pin name	Type	Description	Power domain
TDN2_A	AIO	DSI1 lane2 N	AVDD18_MIPITX2
TDP2_A	AIO	DSI1 lane2 P	AVDD18_MIPITX2
TCN_A	AIO	DSI1 CK lane N	AVDD18_MIPITX2
TCP_A	AIO	DSI1 CK lane P	AVDD18_MIPITX2
TDN1_A	AIO	DSI1 lane1 N	AVDD18_MIPITX2
TDP1_A	AIO	DSI1 lane1 P	AVDD18_MIPITX2
TDN0_A	AIO	DSI1 lane0 N	AVDD18_MIPITX2
TDP0_A	AIO	DSI1 lane0 P	AVDD18_MIPITX2
VRT_A	AO	External resistor for DSI1 bias Connect 1.5K ohm 1% resistor to ground	AVDD18_MIPITX2
PLL			
TN_ARMPLL	AIO	ARMPLL testpin N	AVDD18_ARMPLL
TP_ARMPLL	AIO	ARMPLL testpin P	AVDD18_ARMPLL
TN_MEMPLL_A	AIO	MEMPLL testpin N	AVDD18_MEMPLL_A
TP_MEMPLL_A	AIO	MEMPLL testpin P	AVDD18_MEMPLL_A
TN_MEMPLL_B	AIO	MEMPLL testpin N	AVDD18_MEMPLL_B
TP_MEMPLL_B	AIO	MEMPLL testpin P	AVDD18_MEMPLL_B
TN_MEMPLLPOP	AIO	MEMPLL testpin N	AVDD18_MEMPLLPOP
TP_MEMPLLPOP	AIO	MEMPLL testpin P	AVDD18_MEMPLLPOP
Analog Power/Ground			
AVDD10_SSUSB	P	Analog power 1.0V for SSUSB	
AVDD18_AP	P	Analog power input 1.8V for AuxADC, TSENSE	
AVDD18_ARMPLL	P	Analog power input 1.8V for ARMPLL	
AVDD18_MD	P	Analog power input 1.8V for BBTX, BBRX	
AVDD18_MEMPLL_A	P	Analog power input 1.8V for MEMPLL	
AVDD18_MEMPLL_B	P	Analog power input 1.8V for MEMPLL	
AVDD18_MEMPLLPOP	P	Analog power input 1.8V for MEMPLL	
AVDD18_MIPIRX0	P	Analog power for MIPI CSI	
AVDD18_MIPIRX1	P	Analog power for MIPI CSI	
AVDD18_MIPIRX2	P	Analog power for MIPI CSI	
AVDD18_MIPITX1	P	Analog power for MIPI DSI	
AVDD18_MIPITX2	P	Analog power for MIPI DSI	
AVDD18_PLLGP	P	Analog power input 1.8V for PLL	
AVDD18_SSUSB	P	Analog power 1.8V for SSUSB	
AVDD18_USB_P0	P	Analog power 1.8V for USB	
AVDD18_USB_P1	P	Analog power 1.8V for USB	
AVDD28_DAC	P	Analog power input 2.8V for APC	
AVDD33_USB_P0	P	Analog power 3.3V for USB	
AVDD33_USB_P1	P	Analog power 3.3V for USB	
AVSS10_SSUSB	P	Analog ground 1.0V for SSUSB	
AVSS10_SSUSB	P	Analog ground 1.0V for SSUSB	
AVSS18_ARMPLL	P	Analog ground input 1.8V for ARMPLL	

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Pin name	Type	Description	Power domain
AVSS18_MD	P	Analog ground input 1.8V for BBTX, BBRX	
AVSS18_MEMPLL_A	P	Analog ground input 1.8V for MEMPLL	
AVSS18_MEMPLL_B	P	Analog ground input 1.8V for MEMPLL	
AVSS18_MEMPLLPOP	P	Analog ground input 1.8V for MEMPLL	
AVSS18_MIPIRX	P	Analog ground for MIPI CSI	
AVSS18_MIPITX	P	Analog ground for MIPI DSI	
AVSS18_PLLGP	P	Analog ground input 1.8V for PLL	
AVSS33_USB_P0	P	Analog ground 3.3V for USB	
AVSS33_USB_P1	P	Analog ground 3.3V for USB	
DDR Power			
DDRV_A	P	DRAM I/O power	
DDRV_B	P	DRAM I/O power	
DDRVPOP	P	DRAM I/O power	
EXTDN_A		DRAM REXTDN pin	
VBIASN1_A	P	DRAM VBIASN power	-
VBIASN1_B	P	DRAM VBIASN power	-
VBIASNPOP	P	DRAM VBIASN power	-
VDD1	P	DRAM VDD1 core power	-
VDDQ	P	DRAM I/O power	-
VREF(CA)_A	P	DRAM VREF(CA) power	-
VREF(CA)_B	P	DRAM VREF(CA) power	-
VREF(DQ)_A	P	DRAM VREF(DQ) power	-
VREF(DQ)_B	P	DRAM VREF(DQ) power	-
VREF_A	P	DRAM VREF power	-
VREF_B	P	DRAM VREF power	-
ZQ0_A		DRAM channel A reference pin 0 for output drive strength calibration	
ZQ0_B		DRAM channel B reference pin 0 for output drive strength calibration	
ZQ1_A		DRAM channel A reference pin 1 for output drive strength calibration	
ZQ1_B		DRAM channel B reference pin 0 for output drive strength calibration	
DDR IO			
CAPOP0_A	DIO	DRAM channel A address output 0	DDRVPOP
CAPOP1_A	DIO	DRAM channel A address output 1	DDRVPOP
CAPOP2_A	DIO	DRAM channel A address output 2	DDRVPOP
CAPOP3_A	DIO	DRAM channel A address output 3	DDRVPOP
CAPOP4_A	DIO	DRAM channel A address output 4	DDRVPOP
CAPOP5_A	DIO	DRAM channel A address output 5	DDRVPOP
CAPOP6_A	DIO	DRAM channel A address output 6	DDRVPOP
CAPOP7_A	DIO	DRAM channel A address output 7	DDRVPOP
CAPOP8_A	DIO	DRAM channel A address output 8	DDRVPOP
CAPOP9_A	DIO	DRAM channel A address output 9	DDRVPOP

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Pin name	Type	Description	Power domain
CKEPOP0_A	DIO	DRAM channel A command output CKE 0	DDRVPOP
CKEPOP1_A	DIO	DRAM channel A command output CKE 1	DDRVPOP
CLKPOP_C_A	DIO	DRAM channel A clock 0 output	DDRVPOP
CLKPOP_T_A	DIO	DRAM channel A clock 0 output #	DDRVPOP
CSPOP0_N_A	DIO	DRAM channel A chip select 0 #	DDRVPOP
CSPOP1_N_A	DIO	DRAM channel A chip select 1 #	DDRVPOP
DQ0_A	DIO	DRAM channel A data pin 0	DDRV_A
DQ1_A	DIO	DRAM channel A data pin 1	DDRV_A
DQ10_A	DIO	DRAM channel A data pin 10	DDRV_A
DQ11_A	DIO	DRAM channel A data pin 11	DDRV_A
DQ12_A	DIO	DRAM channel A data pin 12	DDRV_A
DQ13_A	DIO	DRAM channel A data pin 13	DDRV_A
DQ14_A	DIO	DRAM channel A data pin 14	DDRV_A
DQ15_A	DIO	DRAM channel A data pin 15	DDRV_A
DQ16_A	DIO	DRAM channel A data pin 16	DDRV_A
DQ17_A	DIO	DRAM channel A data pin 17	DDRV_A
DQ18_A	DIO	DRAM channel A data pin 18	DDRV_A
DQ19_A	DIO	DRAM channel A data pin 19	DDRV_A
DQ2_A	DIO	DRAM channel A data pin 2	DDRV_A
DQ20_A	DIO	DRAM channel A data pin 20	DDRV_A
DQ21_A	DIO	DRAM channel A data pin 21	DDRV_A
DQ22_A	DIO	DRAM channel A data pin 22	DDRV_A
DQ23_A	DIO	DRAM channel A data pin 23	DDRV_A
DQ24_A	DIO	DRAM channel A data pin 24	DDRV_A
DQ25_A	DIO	DRAM channel A data pin 25	DDRV_A
DQ26_A	DIO	DRAM channel A data pin 26	DDRV_A
DQ27_A	DIO	DRAM channel A data pin 27	DDRV_A
DQ28_A	DIO	DRAM channel A data pin 28	DDRV_A
DQ29_A	DIO	DRAM channel A data pin 29	DDRV_A
DQ3_A	DIO	DRAM channel A data pin 3	DDRV_A
DQ30_A	DIO	DRAM channel A data pin 30	DDRV_A
DQ31_A	DIO	DRAM channel A data pin 31	DDRV_A
DQ4_A	DIO	DRAM channel A data pin 4	DDRV_A
DQ5_A	DIO	DRAM channel A data pin 5	DDRV_A
DQ6_A	DIO	DRAM channel A data pin 6	DDRV_A
DQ7_A	DIO	DRAM channel A data pin 7	DDRV_A
DQ8_A	DIO	DRAM channel A data pin 8	DDRV_A
DQ9_A	DIO	DRAM channel A data pin 9	DDRV_A
DQM0_A	DIO	DRAM channel A DQM 0	DDRV_A
DQM1_A	DIO	DRAM channel A DQM 1	DDRV_A
DQM2_A	DIO	DRAM channel A DQM 2	DDRV_A
DQM3_A	DIO	DRAM channel A DQM 3	DDRV_A
DQS0_C_A	DIO	DRAM channel A DQS 0	DDRV_A
DQS0_T_A	DIO	DRAM channel A DQS 0 #	DDRV_A

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Pin name	Type	Description	Power domain
DQS1_C_A	DIO	DRAM channel A DQS 1	DDRV_A
DQS1_T_A	DIO	DRAM channel A DQS 1 #	DDRV_A
DQS2_C_A	DIO	DRAM channel A DQS 2	DDRV_A
DQS2_T_A	DIO	DRAM channel A DQS 2 #	DDRV_A
DQS3_C_A	DIO	DRAM channel A DQS 3	DDRV_A
DQS3_T_A	DIO	DRAM channel A DQS 3 #	DDRV_A
ODT_A	DIO	DRAM channel A command output ODT	DDRV_A
RFU			
CAPOP0_B	DIO	DRAM channel B address output 0	DDRVPOP
CAPOP1_B	DIO	DRAM channel B address output 1	DDRVPOP
CAPOP2_B	DIO	DRAM channel B address output 2	DDRVPOP
CAPOP3_B	DIO	DRAM channel B address output 3	DDRVPOP
CAPOP4_B	DIO	DRAM channel B address output 4	DDRVPOP
CAPOP5_B	DIO	DRAM channel B address output 5	DDRVPOP
CAPOP6_B	DIO	DRAM channel B address output 6	DDRVPOP
CAPOP7_B	DIO	DRAM channel B address output 7	DDRVPOP
CAPOP8_B	DIO	DRAM channel B address output 8	DDRVPOP
CAPOP9_B	DIO	DRAM channel B address output 9	DDRVPOP
CKEPOP0_B	DIO	DRAM channel B command output CKE 0	DDRVPOP
CKEPOP1_B	DIO	DRAM channel B command output CKE 1	DDRVPOP
CLKPOP_C_B	DIO	DRAM channel B clock 0 output	DDRVPOP
CLKPOP_T_B	DIO	DRAM channel B clock 0 output #	DDRVPOP
CSPOP0_N_B	DIO	DRAM channel B chip select 0 #	DDRVPOP
CSPOP1_N_B	DIO	DRAM channel B chip select 1 #	DDRVPOP
DQ0_B	DIO	DRAM channel B data pin 0	DDRV_B
DQ1_B	DIO	DRAM channel B data pin 1	DDRV_B
DQ10_B	DIO	DRAM channel B data pin 10	DDRV_B
DQ11_B	DIO	DRAM channel B data pin 11	DDRV_B
DQ12_B	DIO	DRAM channel B data pin 12	DDRV_B
DQ13_B	DIO	DRAM channel B data pin 13	DDRV_B
DQ14_B	DIO	DRAM channel B data pin 14	DDRV_B
DQ15_B	DIO	DRAM channel B data pin 15	DDRV_B
DQ16_B	DIO	DRAM channel B data pin 16	DDRV_B
DQ17_B	DIO	DRAM channel B data pin 17	DDRV_B
DQ18_B	DIO	DRAM channel B data pin 18	DDRV_B
DQ19_B	DIO	DRAM channel B data pin 19	DDRV_B
DQ2_B	DIO	DRAM channel B data pin 2	DDRV_B
DQ20_B	DIO	DRAM channel B data pin 20	DDRV_B
DQ21_B	DIO	DRAM channel B data pin 21	DDRV_B
DQ22_B	DIO	DRAM channel B data pin 22	DDRV_B
DQ23_B	DIO	DRAM channel B data pin 23	DDRV_B
DQ24_B	DIO	DRAM channel B data pin 24	DDRV_B
DQ25_B	DIO	DRAM channel B data pin 25	DDRV_B
DQ26_B	DIO	DRAM channel B data pin 26	DDRV_B

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Pin name	Type	Description	Power domain
DQ27_B	DIO	DRAM channel B data pin 27	DDRV_B
DQ28_B	DIO	DRAM channel B data pin 28	DDRV_B
DQ29_B	DIO	DRAM channel B data pin 29	DDRV_B
DQ3_B	DIO	DRAM channel B data pin 3	DDRV_B
DQ30_B	DIO	DRAM channel B data pin 30	DDRV_B
DQ31_B	DIO	DRAM channel B data pin 31	DDRV_B
DQ4_B	DIO	DRAM channel B data pin 4	DDRV_B
DQ5_B	DIO	DRAM channel B data pin 5	DDRV_B
DQ6_B	DIO	DRAM channel B data pin 6	DDRV_B
DQ7_B	DIO	DRAM channel B data pin 7	DDRV_B
DQ8_B	DIO	DRAM channel B data pin 8	DDRV_B
DQ9_B	DIO	DRAM channel B data pin 9	DDRV_B
DQM0_B	DIO	DRAM channel B DQM 0	DDRV_B
DQM1_B	DIO	DRAM channel B DQM 1	DDRV_B
DQM2_B	DIO	DRAM channel B DQM 2	DDRV_B
DQM3_B	DIO	DRAM channel B DQM 3	DDRV_B
DQS0_C_B	DIO	DRAM channel B DQS 0	DDRV_B
DQS0_T_B	DIO	DRAM channel B DQS 0 #	DDRV_B
DQS1_C_B	DIO	DRAM channel B DQS 1	DDRV_B
DQS1_T_B	DIO	DRAM channel B DQS 1 #	DDRV_B
DQS2_C_B	DIO	DRAM channel B DQS 2	DDRV_B
DQS2_T_B	DIO	DRAM channel B DQS 2 #	DDRV_B
DQS3_C_B	DIO	DRAM channel B DQS 3	DDRV_B
DQS3_T_B	DIO	DRAM channel B DQS 3 #	DDRV_B
ODT_B	DIO	DRAM channel B command output ODT	DDRV_B
Core Power			
DVDD_CORE1	P	Digital 1.0V power input for core	-
DVDD_CORE2	P	Digital 1.0V power input for core	-
DVDD_DVFS1	P	Digital 1.0V power input for core	-
DVDD_DVFS2	P	Digital 1.0V power input for core	-
DVDD_GPU	P	Digital 1.0V power input for core	-
DVDD_SRAM1	P	Digital 1.0V power input for core	-
DVDD_SRAM2	P	Digital 1.0V power input for core	-
DVDD18_EFUSE	P	EFUSE power	-
DVNWBIAS	P	DVNWBIAS	-
DVSS	G	Ground	-
PAD Power			
VCC18IO	P	Digital 1.8V power input for IO	-
VCC18IO_1	P	Digital 1.8V power input for IO	-
VCC18IO_BPI	P	Digital 1.8V power input for BPI	-
VCC18IO_BPI_1	P	Digital 1.8V power input for BPI	-
VCC18IO_BPI_2	P	Digital 1.8V power input for BPI	-
VCC18IO_CMR	P	Digital 1.8V power input for Camera	-
VCC18IO_CONN	P	Digital 1.8V power input for CONN	-

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Pin name	Type	Description	Power domain
VCC18IO_DPI	P	Digital 1.8V power input for DPI	-
VCC18IO_EINT	P	Digital 1.8V power input for EINT	-
VCC18IO_I2S	P	Digital 1.8V power input for I2S	-
VCC18IO_MC0	P	Digital 1.8V power input for MSDC0	-
VCC18IO_MC1	P	Digital 1.8V power input for MSDC1	-
VCC18IO_MC2	P	Digital 1.8V power input for MSDC2	-
VCC18IO_MC3	P	Digital 1.8V power input for MSDC3	-
VCC18IO_MD1	P	Digital 1.8V power input for MD1	-
VCC18IO_SIM	P	Digital 1.8V power input for SIM	-
VCC18IO_UART	P	Digital 1.8V power input for UART	-
VCC28_EMD	P	Digital 3.3V power input for EINT	-
VCC28IO_BPI	P	Digital 3.3V power input for BPI	-
VCC33IO_MC1	P	Digital 3.3V power input for MSDC1	-
VCC33IO_MC2	P	Digital 3.3V power input for MSDC2	-
VCC33IO_SIM1	P	Digital 3.3V power input for SIM1	-
VCC33IO_SIM2	P	Digital 3.3V power input for SIM2	-

2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-5. Absolute maximum ratings for power supply

Symbol or Pin name	Description	Min.	Max.	Unit
DVDD_CORE1	Digital 1.0V power input for core	0.81	1.15	V
DVDD_CORE2	Digital 1.0V power input for core	0.81	1.15	V
DVDD_DVFS1	Digital 1.0V power input for core	0.72	1.15	V
DVDD_DVFS2	Digital 1.0V power input for core	0.72	1.15	V
DVDD_GPU	Digital 1.0V power input for core	0.81	1.15	V
DVDD_SRAM1	Digital 1.0V power input for core	0.81	1.15	V
DVDD_SRAM2	Digital 1.0V power input for core	0.81	1.15	V
DVDD18_EFUSE	EFUSE power	1.2	3.3	V
DVNWBIAS	DVNWBIAS	-0.2	0.5	V
DVSS	Ground	0	0	V
VCC18IO	Digital 1.8V power input for IO	1.62	1.98	V
VCC18IO_1	Digital 1.8V power input for IO	1.62	1.98	V
VCC18IO_BPI	Digital 1.8V power input for BPI	1.7	1.9	V
VCC18IO_BPI_1	Digital 1.8V power input for BPI	1.62	1.98	V
VCC18IO_BPI_2	Digital 1.8V power input for BPI	1.62	1.98	V
VCC18IO_CMR	Digital 1.8V power input for Camera	1.62	1.98	V
VCC18IO_CONN	Digital 1.8V power input for CONN	1.62	1.98	V
VCC18IO_DPI	Digital 1.8V power input for DPI	1.62	1.95	V
VCC18IO_EINT	Digital 1.8V power input for EINT	1.7	1.9	V

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Symbol or Pin name	Description	Min.	Max.	Unit
VCC18IO_I2S	Digital 1.8V power input for I2S	1.62	1.98	V
VCC18IO_MC0	Digital 1.8V power input for MSDC0	1.62	1.95	V
VCC18IO_MC1	Digital 1.8V power input for MSDC1	1.7	1.9	V
VCC18IO_MC2	Digital 1.8V power input for MSDC2	1.7	1.9	V
VCC18IO_MC3	Digital 1.8V power input for MSDC3	1.62	1.98	V
VCC18IO_MD1	Digital 1.8V power input for MD1	1.7	1.9	V
VCC18IO_SIM	Digital 1.8V power input for SIM	1.7	1.9	V
VCC18IO_UART	Digital 1.8V power input for UART	1.62	1.98	V
VCC28_EMD	Digital 3.3V power input for EINT	1.7	3.6	V
VCC28IO_BPI	Digital 3.3V power input for BPI	1.7	3.6	V
VCC33IO_MC1	Digital 3.3V power input for MSDC1	1.7	3.6	V
VCC33IO_MC2	Digital 3.3V power input for MSDC2	1.7	3.6	V
VCC33IO_SIM1	Digital 3.3V power input for SIM1	1.7	3.6	V
VCC33IO_SIM2	Digital 3.3V power input for SIM2	1.7	3.6	V
AVDD10_SSUSB	Analog power	0.9	1.1	V
AVDD18_AP	Analog power	1.62	1.98	V
AVDD18_ARMPLL	Analog power	1.62	1.98	V
AVDD18_MD	Analog power	1.62	1.98	V
AVDD18_MEMPLL_A	Analog power	1.62	1.98	V
AVDD18_MEMPLL_B	Analog power	1.62	1.98	V
AVDD18_MEMPLLPOP	Analog power	1.62	1.98	V
AVDD18_MIPIRX0	Analog power	1.62	1.98	V
AVDD18_MIPIRX1	Analog power	1.62	1.98	V
AVDD18_MIPIRX2	Analog power	1.62	1.98	V
AVDD18_MIPITX1	Analog power	1.62	1.98	V
AVDD18_MIPITX2	Analog power	1.62	1.98	V
AVDD18_PLLGP	Analog power	1.62	1.98	V
AVDD18_SSUSB	Analog power	1.62	1.98	V
AVDD18_USB_P0	Analog power	1.62	1.98	V
AVDD18_USB_P1	Analog power	1.62	1.98	V
AVDD28_DAC	Analog power	2.52	3.08	V
AVDD33_USB_P0	Analog power	2.97	3.63	V
AVDD33_USB_P1	Analog power	2.97	3.63	V
DDRV_A	DRAM I/O power	1.14	1.3	V
DDRV_B	DRAM I/O power	1.14	1.3	V
DDRVPOP	DRAM I/O power	1.14	1.3	V
VBIASN1_A	DRAM VBIASN power	0.2	0.2	V
VBIASN1_B	DRAM VBIASN power	0.2	0.2	V
VBIASNPOP	DRAM VBIASN power	0.2	0.2	V
VDD1	DRAM VDD1 core power	1.7	1.95	V
VDDQ	DRAM I/O power	1.14	1.3	V
VREF(CA)_A	DRAM VREF(CA) power	0.588	0.612	V
VREF(CA)_B	DRAM VREF(CA) power	0.588	0.612	V

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Symbol or Pin name	Description	Min.	Max.	Unit
VREF(DQ)_A	DRAM VREF(DQ) power	0.588	0.612	V
VREF(DQ)_B	DRAM VREF(DQ) power	0.588	0.612	V
VREF_A	DRAM VREF power	0.588	0.612	V
VREF_B	DRAM VREF power	0.588	0.612	V

Warning: Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.

2.2.2 Recommended Operating Conditions

Table 2-6. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD_CORE1	Digital 1.0V power input for core	0.81	1.125	1.15	V
DVDD_CORE2	Digital 1.0V power input for core	0.81	1.125	1.15	V
DVDD_DVFS1	Digital 1.0V power input for core	0.72	1.1	1.15	V
DVDD_DVFS2	Digital 1.0V power input for core	0.72	1.125	1.15	V
DVDD_GPU	Digital 1.0V power input for core	0.81	1.125	1.15	V
DVDD_SRAM1	Digital 1.0V power input for core	0.81	1.1	1.15	V
DVDD_SRAM2	Digital 1.0V power input for core	0.81	1.125	1.15	V
DVDD18_EFUSE	EFUSE power	1.2	1.8	3.3	V
DVNWBIAS	DVNWBIAS	-0.2	0.3	0.5	V
DVSS	Ground	0	0	0	V
VCC18IO	Digital 1.8V power input for IO	1.7	1.8	1.98	V
VCC18IO_1	Digital 1.8V power input for IO	1.7	1.8	1.98	V
VCC18IO_BPI	Digital 1.8V power input for BPI	1.7	1.8	1.9	V
VCC18IO_BPI_1	Digital 1.8V power input for BPI	1.7	1.8	1.98	V
VCC18IO_BPI_2	Digital 1.8V power input for BPI	1.7	1.8	1.98	V
VCC18IO_CMR	Digital 1.8V power input for Camera	1.7	1.8	1.98	V
VCC18IO_CONN	Digital 1.8V power input for CONN	1.7	1.8	1.98	V
VCC18IO_DPI	Digital 1.8V power input for DPI	1.7	1.8	1.95	V
VCC18IO_EINT	Digital 1.8V power input for EINT	1.7	1.8	1.9	V
VCC18IO_I2S	Digital 1.8V power input for I2S	1.7	1.8	1.98	V
VCC18IO_MC0	Digital 1.8V power input for MSDC0	1.7	1.8	1.95	V
VCC18IO_MC1	Digital 1.8V power input for MSDC1	1.7	1.8	1.9	V
VCC18IO_MC2	Digital 1.8V power input for MSDC2	1.7	1.8	1.9	V
VCC18IO_MC3	Digital 1.8V power input for MSDC3	1.7	1.8	1.98	V
VCC18IO_MD1	Digital 1.8V power input for MD1	1.7	1.8	1.9	V
VCC18IO_SIM	Digital 1.8V power input for SIM	1.7	1.8	1.9	V
VCC18IO_UART	Digital 1.8V power input for UART	1.7	1.8	1.98	V
VCC28_EMD	Digital 3.3V power input for EINT	2.7	3.3	3.6	V
		1.7	1.8	1.9	
VCC28IO_BPI	Digital 3.3V power input for BPI	2.7	3.3	3.6	V
		1.7	1.8	1.9	

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VCC33IO_MC1	Digital 3.3V power input for MSDC1	2.7	3.3	3.6	V
		1.7	1.8	1.9	
VCC33IO_MC2	Digital 3.3V power input for MSDC2	2.7	3.3	3.6	V
		1.7	1.8	1.9	
VCC33IO_SIM1	Digital 3.3V power input for SIM1	2.7	3.3	3.6	V
		1.7	1.8	1.9	
VCC33IO_SIM2	Digital 3.3V power input for SIM2	2.7	3.3	3.6	V
		1.7	1.8	1.9	
AVDD10_SSUSB	Analog power	0.95	1.0	1.05	V
AVDD18_AP	Analog power	1.71	1.8	1.89	V
AVDD18_ARMPLL	Analog power	1.71	1.8	1.89	V
AVDD18_MD	Analog power	1.71	1.8	1.89	V
AVDD18_MEMPLL_A	Analog power	1.71	1.8	1.89	V
AVDD18_MEMPLL_B	Analog power	1.71	1.8	1.89	V
AVDD18_MEMPLLPOP	Analog power	1.71	1.8	1.89	V
AVDD18_MIPIRX0	Analog power	1.71	1.8	1.89	V
AVDD18_MIPIRX1	Analog power	1.71	1.8	1.89	V
AVDD18_MIPIRX2	Analog power	1.71	1.8	1.89	V
AVDD18_MIPITX1	Analog power	1.71	1.8	1.89	V
AVDD18_MIPITX2	Analog power	1.71	1.8	1.89	V
AVDD18_PLLGP	Analog power	1.71	1.8	1.89	V
AVDD18_SSUSB	Analog power	1.71	1.8	1.89	V
AVDD18_USB_P0	Analog power	1.71	1.8	1.89	V
AVDD18_USB_P1	Analog power	1.71	1.8	1.89	V
AVDD28_DAC	Analog power	2.66	2.8	2.94	V
AVDD33_USB_P0	Analog power	3.135	3.3	3.465	V
AVDD33_USB_P1	Analog power	3.135	3.3	3.465	V
DDRV_A	DRAM I/O power	1.14	1.2	1.3	V
DDRV_B	DRAM I/O power	1.14	1.2	1.3	V
DDRVPOP	DRAM I/O power	1.14	1.2	1.3	V
VBIASN1_A	DRAM VBIASN power	0.2	0.2	0.2	V
VBIASN1_B	DRAM VBIASN power	0.2	0.2	0.2	V
VBIASNPOP	DRAM VBIASN power	0.2	0.2	0.2	V
VDD1	DRAM VDD1 core power	1.7	1.8	1.95	V
VDDQ	DRAM I/O power	1.14	1.2	1.3	V
VREF(CA)_A	DRAM VREF(CA) power	0.588	0.6	0.612	V
VREF(CA)_B	DRAM VREF(CA) power	0.588	0.6	0.612	V
VREF(DQ)_A	DRAM VREF(DQ) power	0.588	0.6	0.612	V
VREF(DQ)_B	DRAM VREF(DQ) power	0.588	0.6	0.612	V
VREF_A	DRAM VREF power	0.588	0.6	0.612	V
VREF_B	DRAM VREF power	0.588	0.6	0.612	V

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2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After bag opened, devices subject to infrared reflow, vapor-phase reflow, or equivalent processing must be:
   - Mounted within 168 hours at factory conditions of ≤ 30°C/60% RH, or
   - Stored at ≤ 20% RH.
3. Devices require baking, before mounting, if:
   - 192 hours at 40°C +5°C/-0°C and < 5% RH for low temperature device containers, or
   - 24 hours at 125°C +5°C/-0°C for high temperature device containers.

2.2.4 AC Electrical Characteristics and Timing Diagram

2.2.4.1 External Memory Interface for LPDDR3

The external memory interface, shown in Figure 2-3, Figure 2-4 and Figure 2-5, is used to connect LPDDR3 device for MT6595. It includes pins CLK_T, CLK_C, CKE[1:0], CS[1:0], DQS[3:0], DQS#[3:0], CA[9:0] and DQ[31:0]. Table 2-7 summarizes the symbol definition and the related timing specifications.

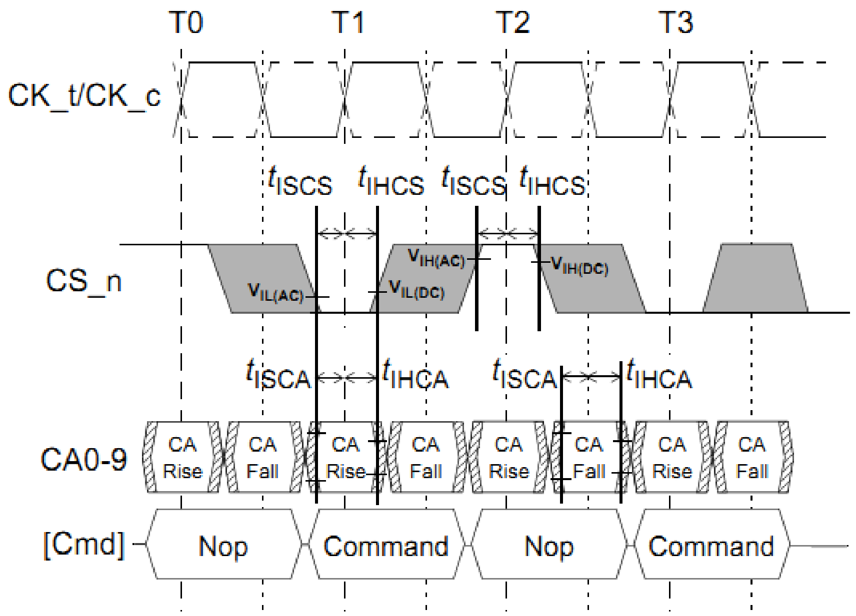

Figure 2-3. Basic timing parameter for LPDDR3 commands

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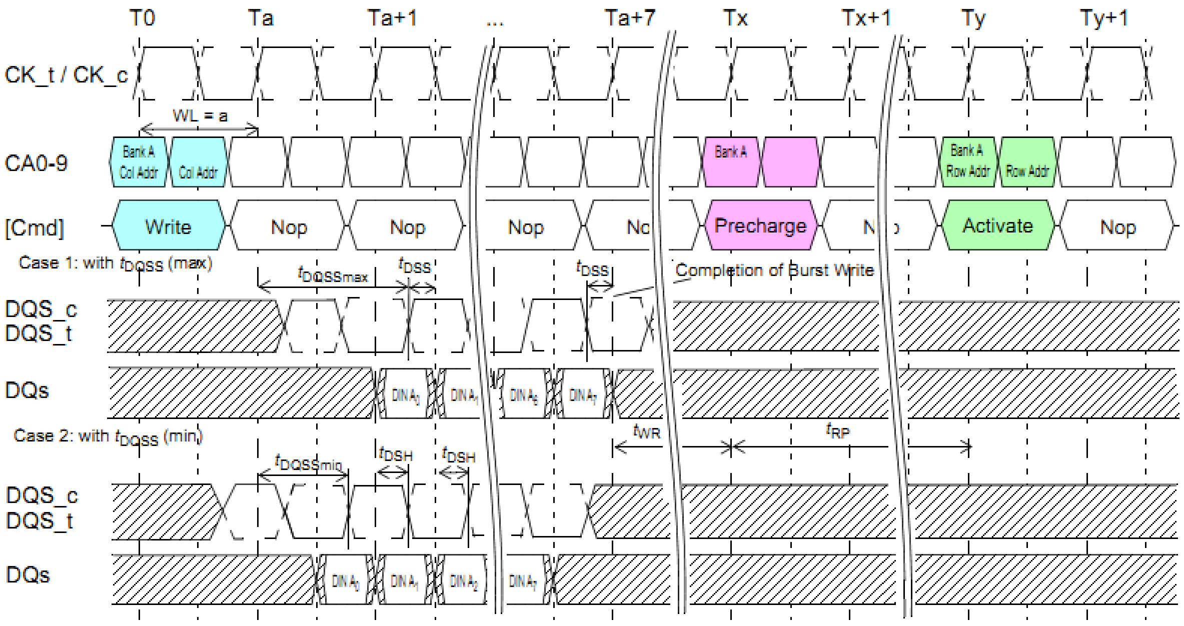

Figure 2-4. Basic timing parameter for LPDDR3 write

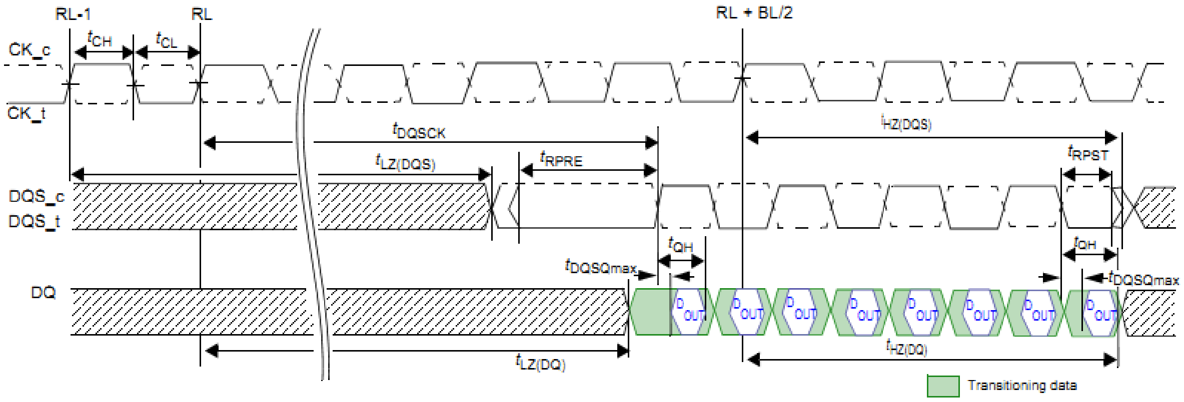

Figure 2-5. Basic LPDDR3 read timing parameter.

Table 2-7. LPDDR3 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	1.071		100	ns
tDQSCK	DQS output access time from CK/CK'	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.13			ns
tDH	DQ & DM input hold time	0.13			ns

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Symbol	Description	Min.	Typ.	Max.	Unit
tDIPW	DQ and DM input pulse width	0.35			tCK
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK
tWPST	Write postamble	0.4			tCK
tWPRE	Write preamble	0.8			tCK
tISCA	Address & control input setup time	0.13			ns
tIHCA	Address & control input hold time	0.13			ns
tISCS	CS_ input setup time	0.23			ns
tIHCS	CS_ input hold time	0.23			ns
tIPWCA	Address and control input pulse width	0.35			tCK
tIPWCS	CS_ input pulse width	0.7			tCK
tCKE	CKE minimum pulse width (HIGH and LOW pulse width)	max(7.5ns, 3tCK)			ns
tISCKE	CKE input setup time	0.25			tCK
tIHCKE	CKE input hold time	0.25			tCK
tCPDED	Command path disable delay	2			tCK
tLZ(DQS)	DQS low-impedance time from CK/CK'	tDQSCK(MIN) - 0.3			ns
tHZ(DQS)	DQS high-impedance time from CK/CK'			tDQSCK (MAX) – 0.1	ns
tLZ(DQ)	DQ low-impedance time from CK/CK'	tDQSCK(MIN) - 0.3			ns
tHZ(DQ)	DQ high-impedance time from CK/CK'			tDQSCK(MAX) + (1.4 × tDQSQ(MAX))	ns
tDQSQ	DQS-DQ skew			0.115	ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH - 0.05			tCK
tQSL	DQS output low pulse width	tCL - 0.05			tCK
tQH	DQ/DQS output hold time from DQS	min(tQSH, tQSL)			ns
tMRW	MODE register Write command period	Max(10tCK, 15)			ns
tMRR	MODE register Read command period	4			tCK
tMRD	Mode register set command delay	Max(10tCK,			ns

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Symbol	Description	Min.	Typ.	Max.	Unit
		14)			
tRPRE	Read preamble	0.9			tCK
tRPST	Read postamble	0.3			tCK
tRAS	ACTIVE to PRECHARGE command period	Max(42ns, 3tCK)		70000	ns
tRC	ACTIVE to ACTIVE command period	tRAS + tRPab (with all-bank pre-charge) tRAS + tRPpb (with per-bank pre-charge)			ns
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			ns
tRCD	ACTIVE to READ or WRITE delay	Max (18ns, 3tCK)			ns
tRPpb	Row PRECHARGE Time (single bank)	Max (18ns, 3tCK)			ns
tRPab	Row PRECHARGE Time (all banks)	Max (21ns, 3tCK)			ns
tRRD	ACTIVE bank A to ACTIVE bank B delay	Max(10ns, 2tCK)			ns
tWR	WRITE recovery time	Max(15ns, 4tCK)			ns
tWTR	Internal write to READ command time	Max(7.5ns, 4tCK)			ns
tXSR	SELF REFRESH exit to next valid command	Max (tRFCab + 10ns, 2tCK)			ns
tXP	EXIT power down to next valid command delay	Max(7.5ns, 3tCK)			ns
tREFW	Refresh Period			32	ms
tRFCab	Refresh Cycle time	130			Ns
tRFCpb	Per Bank Refresh Cycle time	60			ns
tRTP	Internal READ to PRECHARGE command delay	Max(7.5ns, 4tCK)			ns
tCCD	CAS-to-CAS delay	4			tCK

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2.3 System Configuration

2.3.1 Mode Selection

Table 2-8. Mode selection of chip

Pin name	Description
KP_COL0	0: Trigger USB download without battery 1: NA
KP_ROW0	0: Trigger USB download without battery 1: NA

2.3.2 Constant Tied Pins

Table 2-9. Constant tied pins of chip

Pin name	Description
TESTMODE	Test mode (tied to GND)

2.4 Power-on Sequence

The power-on/off sequence with XTAL is shown in the following figure:

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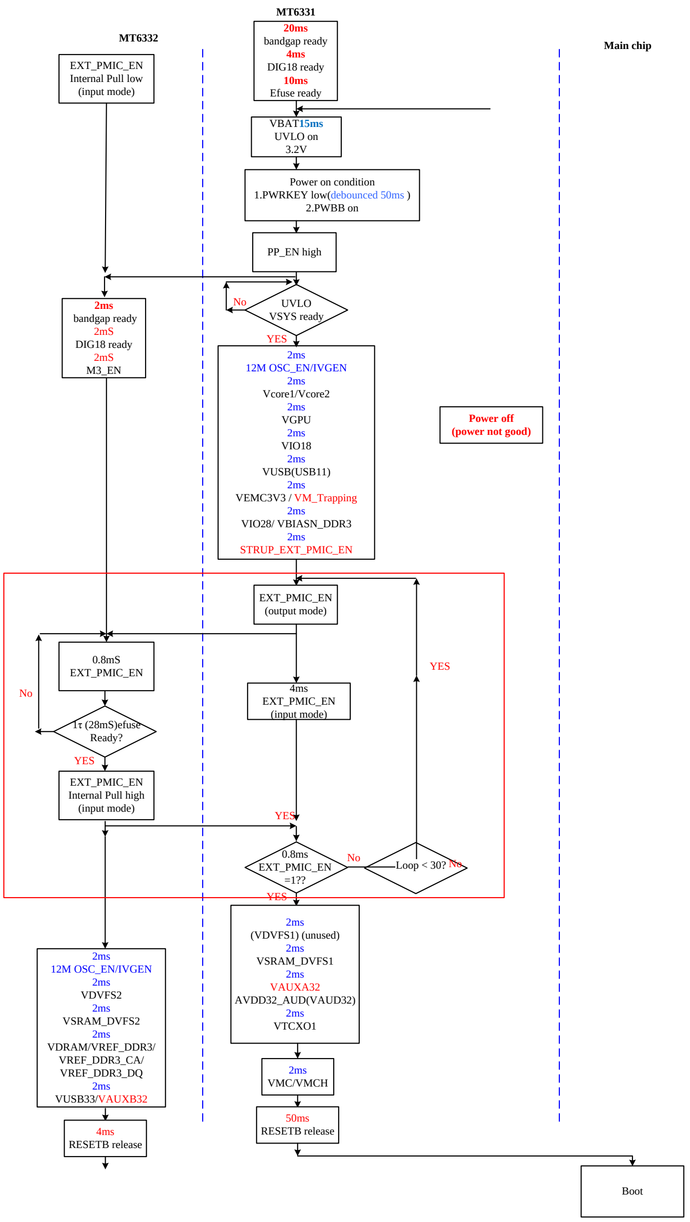

Figure 2-6. Power on/off sequence with XTAL

2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control.

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During the writing or reading of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE base-band signal processing:

Base-band Rx: For I/Q channels base-band A/D conversion
Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
ETDAC: A DAC output to control buck-converter for envelop tracking technique.
RF control: Two DACs for automatic power control (APC) is included.The outputs are provided to external RF power amplifiers respectively.
Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring.
Clock generation: One clock-squarer for shaping the input sinwave clock and 20 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- LTE_BBRX
- TD_BBRX
- BBTX
- ETDAC
- APC-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 LTE_BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
2. A/D converter: 4 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

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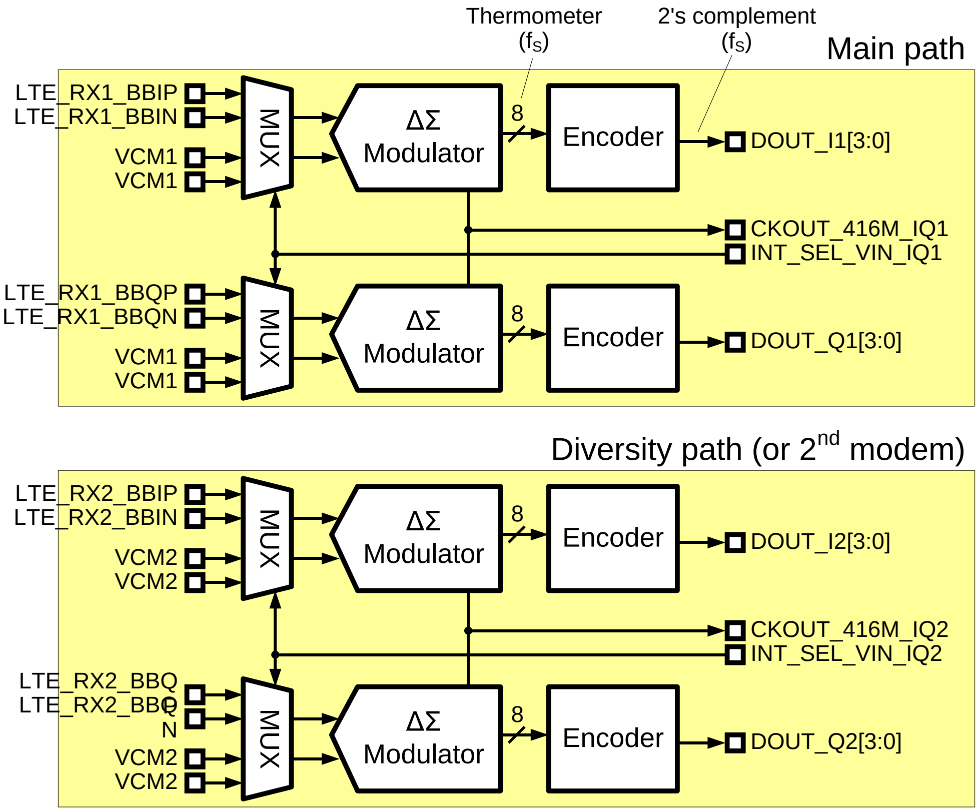

Figure 2-7. Block diagram of LTE_BBRX-ADC

2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-10. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency – Clock rate (LTE HB mode) – Clock rate (LTE LB mode) – Clock rate (DC mode) – Clock rate (SC mode & GSM mode)		 416 208 416 208		MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter, DC mode			0.14	% (rms)

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input clock period jitter, SC mode & GSM mode			0.61	% (rms)
RIN	Differential input resistance – LTE HB mode – LTE LB mode – DC mode – SC mode & GSM mode	2.8 5.6 5.6 11.2	4 8 8 16	5.2 10.4 10.4 20.8	kΩ
FS	Output sampling rate		416/208		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise – LTE HB mode, 2.4Vpp (10.2MHz) sinewave, 1kHz ~ 9MHz band – LTE LB mode, 2.4Vpp (5.2MHz) sinewave, 1kHz ~ 4.5MHz band – DC mode, 2.4Vpp (5.2MHz) sinewave, 400kHz ~ 4.6MHz band – SC mode, 2.4Vpp (2.7MHz) sinewave, 1kHz ~ 2.1MHz band – GSM mode: 2.4Vpp(570kHz) sinewave, 70kHz ~ 270kHz band	68 68 72 72 84	71 71 75 75 87		dB dB dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down			4.5 1	mA uA

2.5.3.2 TD_BBRX

2.5.3.2.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

3. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
4. A/D converter: 2 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

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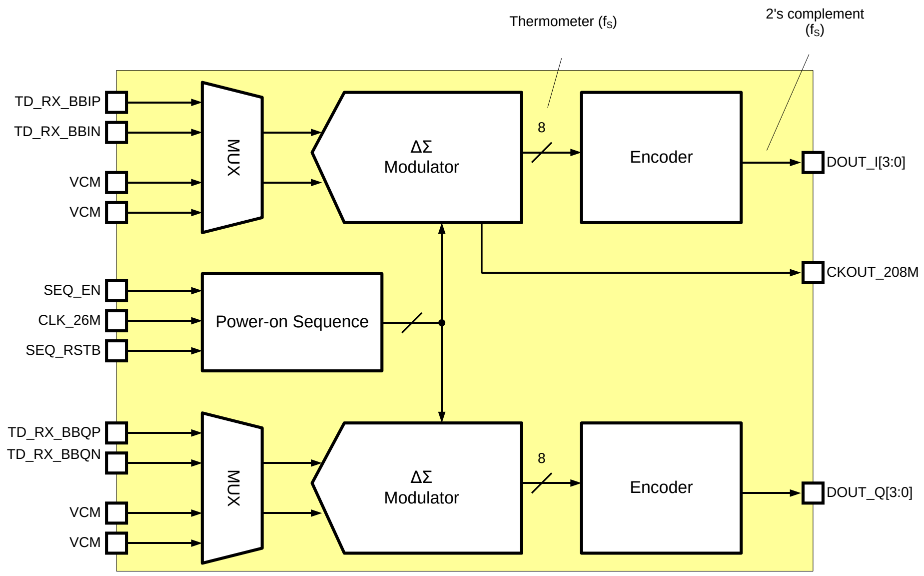

Figure 2-8: Block diagram of TD_BBRX-ADC

2.5.3.3 Function Specifications

See the table below for the function specifications of the base-band downlink receiver.

Table 2-11: Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.7	0.75	0.8	V
FC	Clock rate		208		MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter			0.61	% (rms)
RIN	Differential input resistance	11.2	16	20.8	kΩ
FS	Output sampling rate		208		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise – 2.4Vpp (1.6MHz) sinewave, 1KHz ~ 640KHz band	75	78		dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down			2 1	mA uA

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2.5.3.4 LTE_BBTX

2.5.3.4.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 11-bit which is encoded into 7 bits of thermometer code and 8 binary code by digital hard macro inside BBTX layout. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

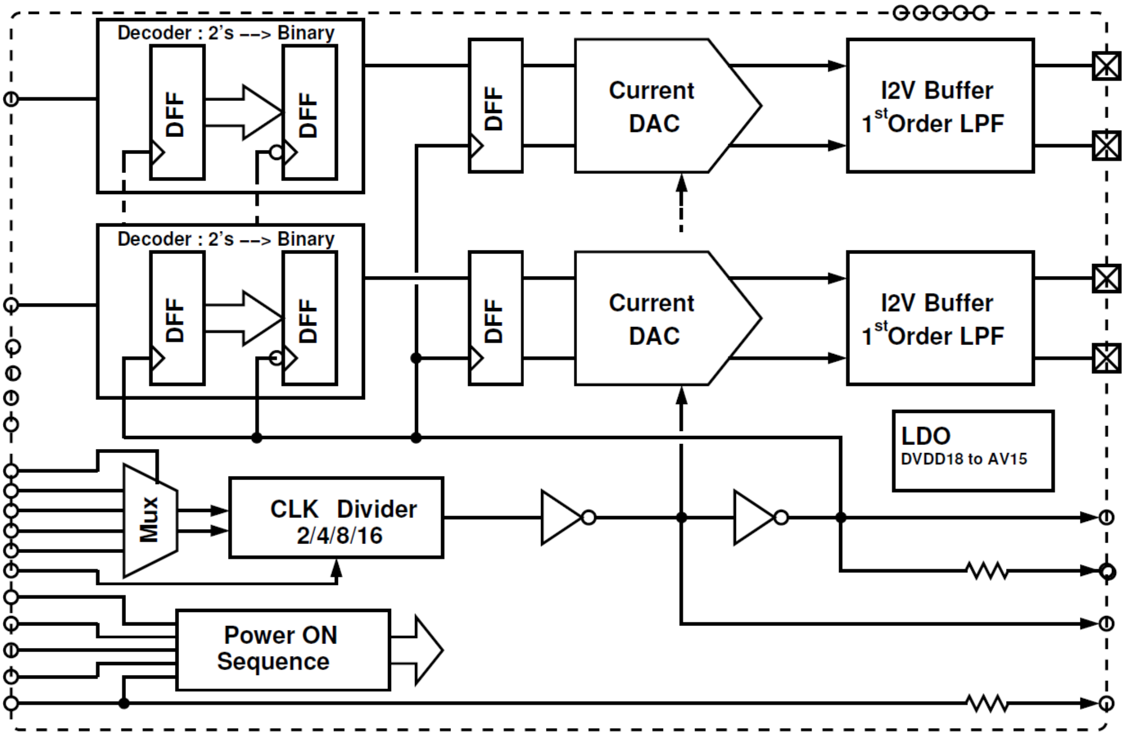

Figure 2-9. Block diagram of LTE_BBTX

2.5.3.4.2 Functional Specifications

Table 2-12. LTE_BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
I_K	HF leakage current @ supply, Irms @416*2 = 832MHz			3.5	uA

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Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		11.0		bit
F_s	Sampling clock		416		MHz
I_{mis}	1-sgma DAC unit cell mismatch			1	%
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os}	3-sigma output differential DC offset			20	mV
F_{3dB}	3dB corner freq.		20/40		MHz
N_{OOB}	Output noise level @25MHz		40		nVrms/sqrt(Hz)
Dinb	Inband Droop		0.1		dB
DNL			1		LSB
INL			2		LSB
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-58	-55	dBc
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 8 10		 mA uA

2.5.3.5 TD_BBTX

2.5.3.5.1 Block Descriptions

BBTX includes two channels of DACs with the first order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current, and the active RC filter performs current to the voltage buffer.

The bitwidth of DACs is 10-bit which is encoded into 7 bits of thermometer code and 7 binary code by mixedsys hardware. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. MD-PLL deliver 832MHz differential clock to BBTX. A clock divider translates 832MHz to 416MHz for DACs and AFIFO inside the mixedsys.

The IO power, DVDD18_MD, is regulated to a voltage around 1.55V to supply analog component, and the required bias currents are generated by BBRX.

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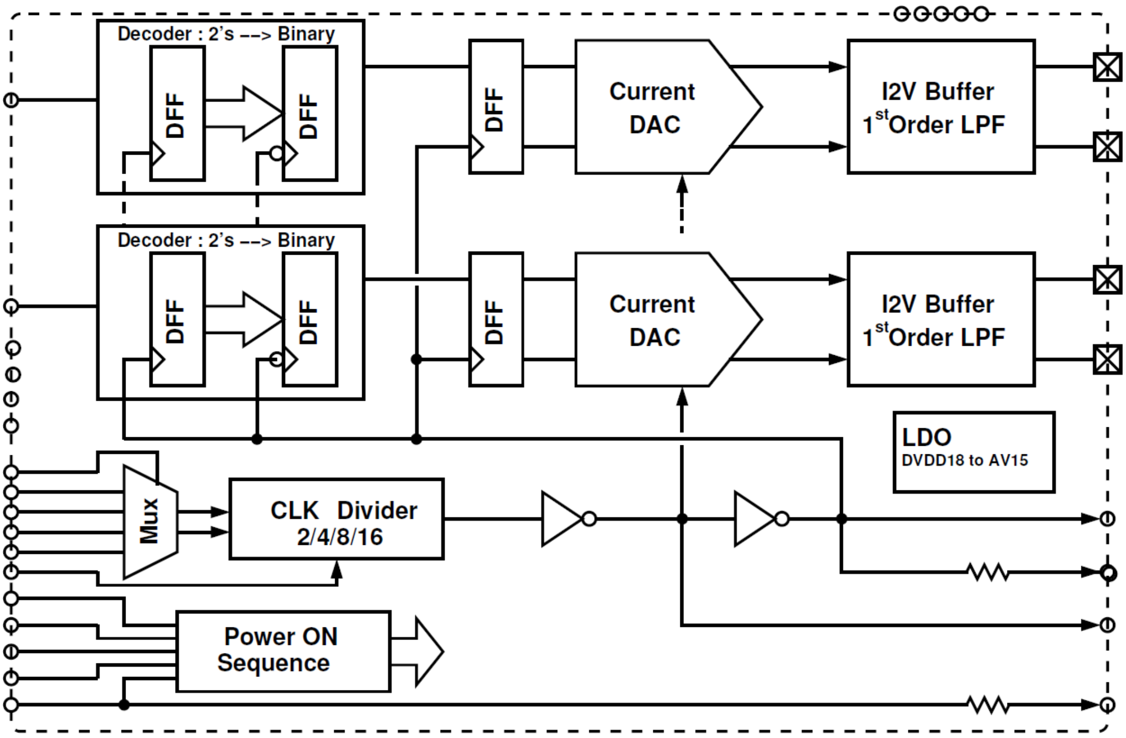

Figure 2-10. Block diagram of TD_BBTX

2.5.3.5.2 Functional Specifications

Table 2-13. TD_BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit.
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
I_K	HF Leakage current @ supply, Irms @416*2=832MHz			3.5	uA
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		10.0		bit
F_s	Sampling clock		416		MHz
I_{mis}	1-sgma DAC unit cell mismatch			1	%
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os_T}	3-sigma output differential DC offset over temp.			4	mV
V_{os}	3-sigma output differential DC offset			10	mV
F_{3dB}	3dB corner freq.	20	25	30	MHz
S_{LPF}	LPF selectivity @832MHz	28			dB
N_{OOB}	Output noise level @45MHz		15.1	30.1.	nVrms/sqrt(Hz)

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Symbol	Parameter	Min.	Typ.	Max.	Unit.
CN	Signal to noise ratio@45MHz		-146	-140	dBc/Hz
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-60	-56	dBc
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		6.7 10		mA uA

2.5.3.6 ETDAC

2.5.3.6.1 Block Descriptions

The ETDAC (Envelope tracking DAC) provides analog envelope signal to external ET modulator. It includes:

1. 11-bit D/A converter: Converts digital modulated signals to analog domain. The input to the DAC is sampled at 416 MHz rate with the 11-bit resolution.
2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 15/30MHz 1st-order Butterworth frequency response.

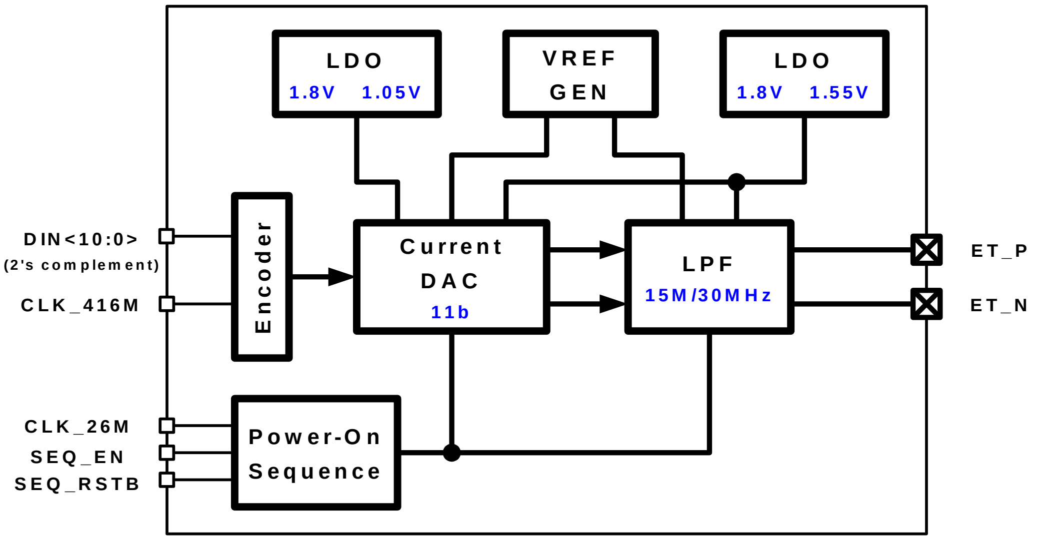

Figure 2-11. Block diagram of ETDAC

2.5.3.6.2 Function Specfications

Table 2-14. ETDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit

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Symbol	Parameter	Min.	Typ.	Max.	Unit
FS	Sampling rate		416		MSPS
IM3	3rd order Intermodulation distortion		-60	-50	dB
	Output swing (full Swing)		2		Vppd
VOCM	Output CM voltage	0.6		0.85	V
	Output capacitance (single-ended)			10	PF
	Output resistance (differential)		100		KΩ
DNL	Differential nonlinearity	-1		+1	LSB
INL	Integral nonlinearity	-2		+2	LSB
FCUT	Filter -3dB cutoff frequency (calibrated)		15/30		MHz
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 4.5 10		 mA uA

2.5.3.7 APC-DAC

2.5.3.7.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

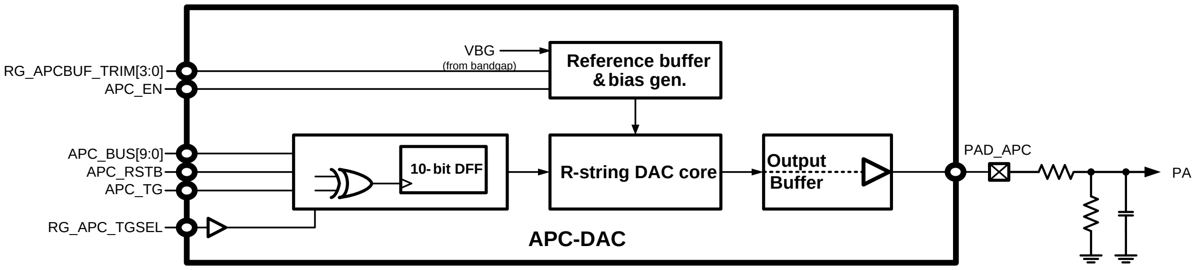

Figure 2-12. Block diagram of APC-DAC

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC.

Table 2-15. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s

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Symbol	Parameter	Min.	Typ.	Max.	Unit
SNDR	Signal-to-noise-and-distortion ratio (10kHz sine wave with 1.0V swing)		50		dB
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		220	2200	pF
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–20		85	°C
I_{ON}	Current consumption (power-on state)		350		uA
I_{OFF}	Current consumption (power-down state)			20	uA

2.5.3.8 AUXADC

2.5.3.8.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measuring and some for external voltage measuring. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

See
Table 2-16. Definitions of AUXADC channels for brief descriptions of AUXADC input channels.

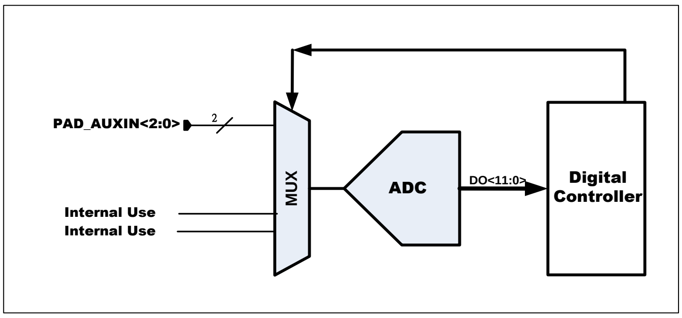

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Figure 2-13. Block diagram of AUXADC

Table 2-16. Definitions of AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)
Channel 1	External use (AUX_IN1)
Channel 2	NA
Channel 3	NA
Channel 4	NA
Channel 5	NA
Channel 6	NA
Channel 7	NA
Channel 8	NA
Channel 9	NA
Channel 10	Internal Use
Channel 11	Internal Use
Channel 12	External use (AUX_IN2)
Channel 13	NA
Channel 14	NA
Channel 15	NA

2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-17. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		4		MHz
FS	Sampling rate @ N-Bit		4/(N+4)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel		50 4		fF pF
RIN	Input resistance Unselected channel	20			MΩ
	Clock latency		N+4		1/FC

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Symbol	Parameter	Min.	Typ.	Max.	Unit
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
SINAD	Signal to noise and distortion ratio (1kHz full swing input & 1.0833MHz clock rate)	62	68		dB
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	1.75	1.8	1.85	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		400 1		uA uA

2.5.3.9 Clock Squarer

2.5.3.9.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.9.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

Table 2-18. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		500		uA

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2.5.3.10 Phase Locked Loop

2.5.3.10.1 Block Descriptions

There are total 18 PLLs in PLL macro, providing several clocks for CPU, BUS, modem, analog modem, MSDC and image-sensor.

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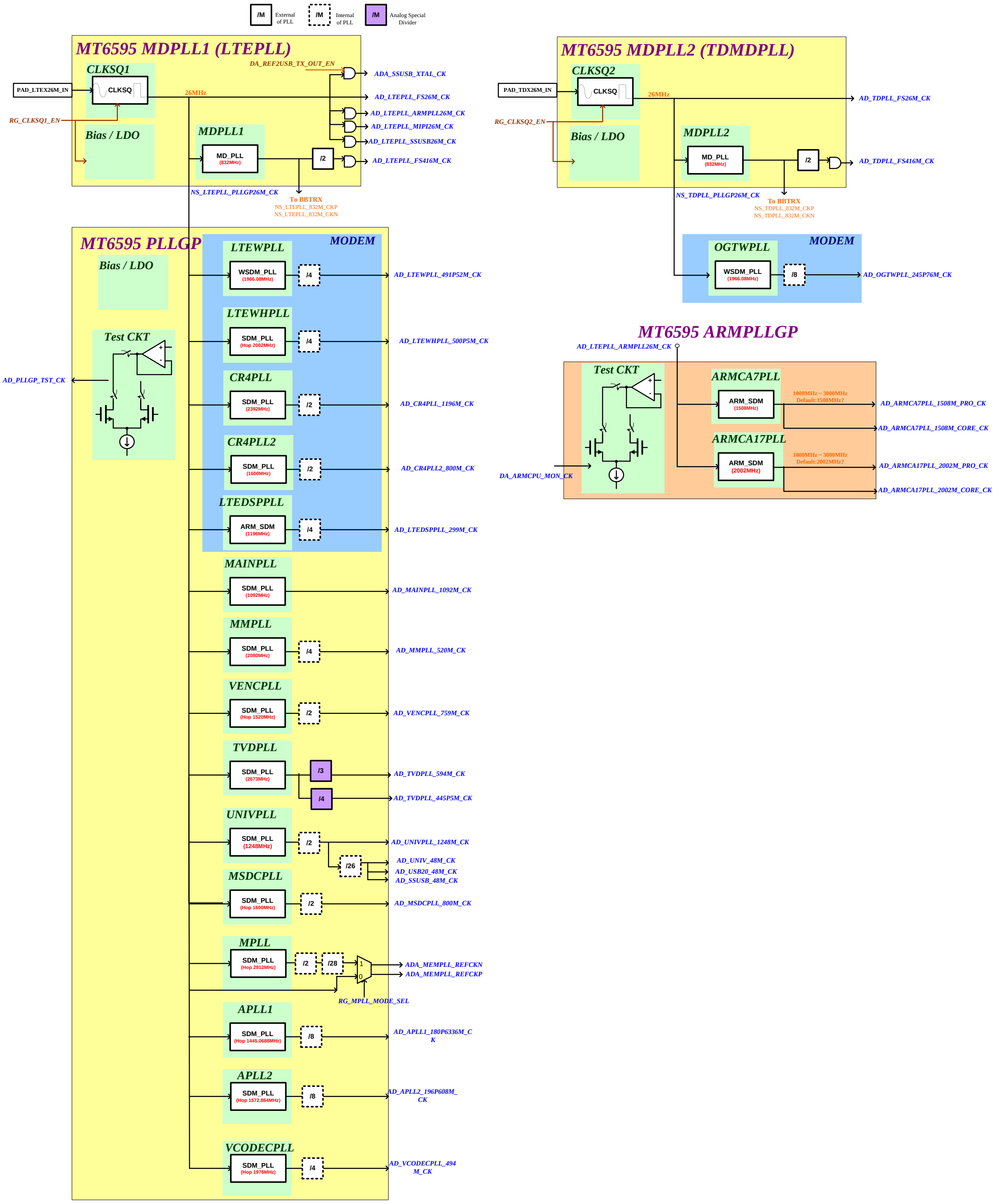

Figure 2-14. Block diagram of PLL

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2.5.3.10.2 Functional Specifications

See the table below for the functional specifications of PLL.

Table 2-19. ARMCA7PLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1508		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1.2		mA
	Power-down current consumption			0.1	uA

Table 2-20. ARMCA17PLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1716		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1.2		mA
	Power-down current consumption			0.1	uA

Table 2-21. MAINPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz

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Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency		1092		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1.2		mA
	Power-down current consumption			0.1	uA

Table 2-22. MMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		351		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-23. UNIVPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	1248	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps

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Symbol	Parameter	Min.	Typ.	Max.	Unit
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-24. MSDCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		800		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-25. MDPLL1 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	416	N/A	MHz
	Settling time		100		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		6.6		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		4.2		mA

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Power-down current consumption			0.3	uA

Table 2-26. MDPLL2 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	416	N/A	MHz
	Settling time		100		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		13.8		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		2.5		mA
	Power-down current consumption			0.2	uA

Table 2-27. LTEWPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	491.52	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-28. LTEWHPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz

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Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency		500.5		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-29. CR4PLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1196		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-30. VENCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		759		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps

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Symbol	Parameter	Min.	Typ.	Max.	Unit
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-31. TVDPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		445.5		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-32. CR4PLL2 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		800		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-33. OGTWPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		245.76		MHz
	Settling time		20		Us

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-34. LTEDSPPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		299		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-35. MPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		52		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-36. APLL1 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		180.6336		MHz

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-37. APLL2 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		196.608		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-38. VCODECPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		494		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

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2.5.3.11 Temperature Sensor

2.5.3.11.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.3.11.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-39. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		60		uA
	Quiescent current		10		uA

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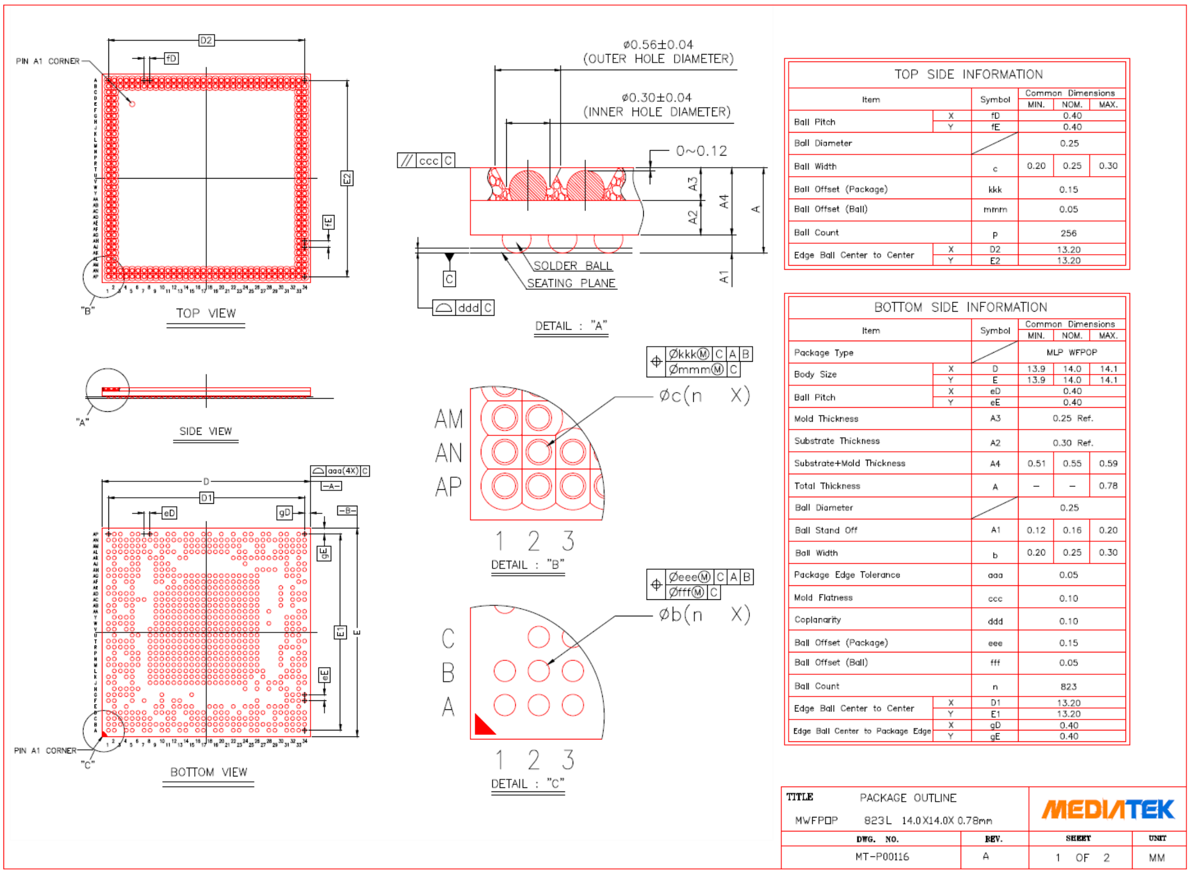
2.6 Package Information

2.6.1 Package Outlines



TOP SIDE INFORMATION					
Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Ball Pitch	X	fD		0.40	
	Y	fE		0.40	
Ball Diameter				0.25	
Ball Width		c	0.20	0.25	0.30
Ball Offset (Package)		kkk		0.15	
Ball Offset (Ball)		mmm		0.05	
Ball Count		p		256	
Edge Ball Center to Center	X	D2		13.20	
	Y	E2		13.20	

BOTTOM SIDE INFORMATION					
Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				MLP WFPOP	
Body Size	X	D	13.9	14.0	14.1
	Y	E	13.9	14.0	14.1
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.25 Ref.	
Substrate Thickness		A2		0.30 Ref.	
Substrate+Mold Thickness		A4	0.51	0.55	0.59
Total Thickness		A	–	–	0.78
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.10	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		823	
Edge Ball Center to Center	X	D1		13.20	
	Y	E1		13.20	
Edge Ball Center to Package Edge	X	gD		0.40	
	Y	gE		0.40	

*Figure 2-15. Outlines and dimensions of WFPOP 14mm*14mm, 823-ball, 0.4mm pitch package*

2.6.2 Thermal Operating Specifications

Table 2-40. Thermal operating specifications

Symbol	Description	Value	Unit	Notes
	Maximum operating junction temperature	125	°C	
	Package thermal resistances in nature convection	25.3	°C/Watt	

2.6.3 Lead-free Packaging

MT6595 is provided in a lead-free package and meets RoHS requirements.

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2.7 Ordering Information

2.7.1 Top Marking Definition

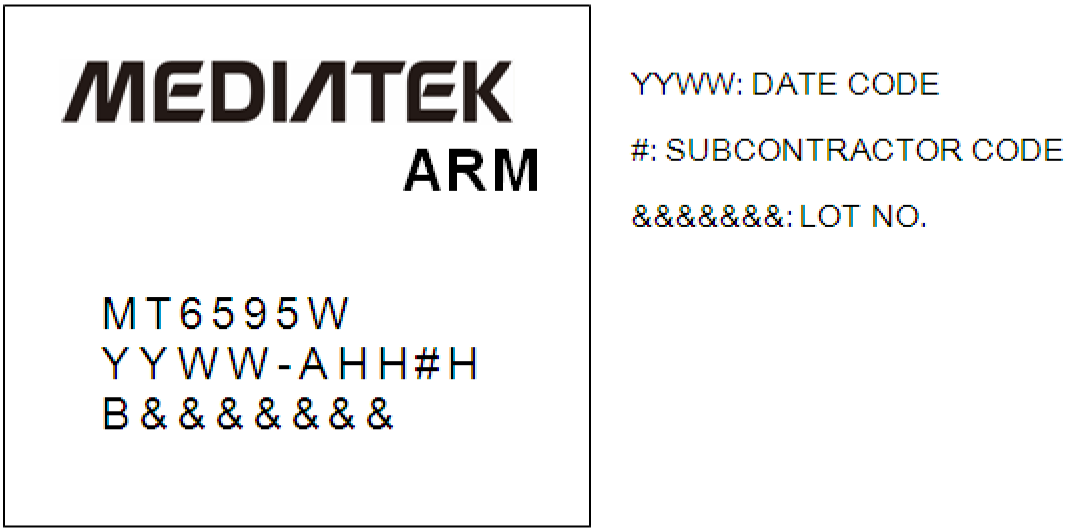

Figure 2-16. Top mark of MT6595

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